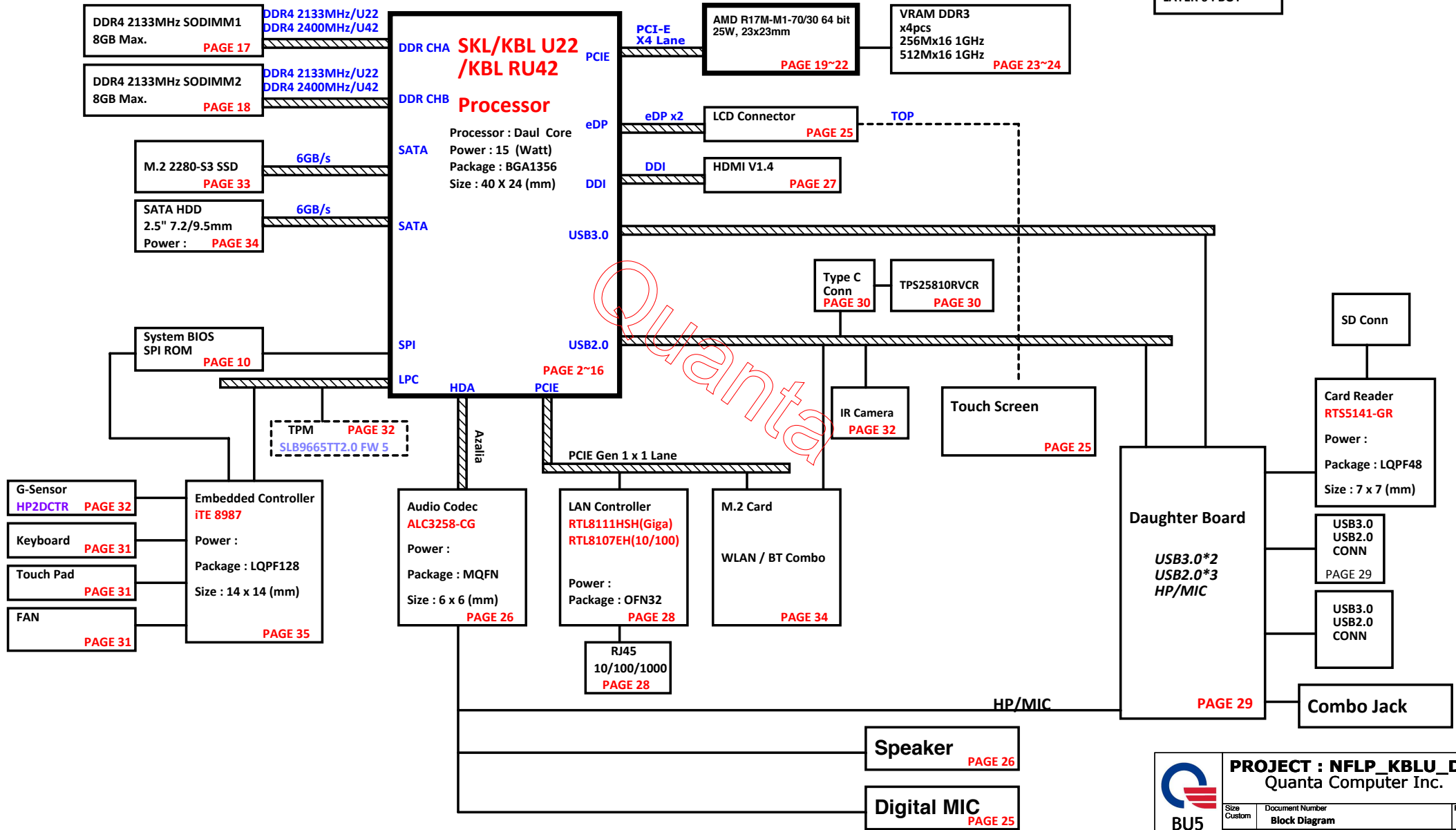


# NFL\_1SPD DIS (14/15")

## Intel SKL/KBL ULT Platform Block Diagram

PCB 6L STACK UP

LAYER 1 : TOP  
LAYER 2 : SGND  
LAYER 3 : IN1(High)  
LAYER 4 : IN2  
LAYER 5 : SVCC  
LAYER 6 : BOT



**PROJECT : NFLP\_KBLU\_DR**  
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
Block Diagram		
Date: Friday, March 24, 2017	Sheet 1 of 49	

+3V 4,10,11,12,13,14,15,17,18,25,26,27,28,29,31,32,33,34,35,41,48  
+1.0V 4,6,35,40  
+VCCSTPLL 4,5,6,9,40,41

## HDMI

27 IN\_D2# IN\_D2# E55  
27 IN\_D2 IN\_D2 F55  
27 IN\_D1# IN\_D1# F58  
27 IN\_D1 IN\_D1 F58  
27 IN\_D0# IN\_D0# G53  
27 IN\_D0 IN\_D0 F56  
27 IN\_CLK# IN\_CLK# G56  
27 IN\_CLK IN\_CLK G56

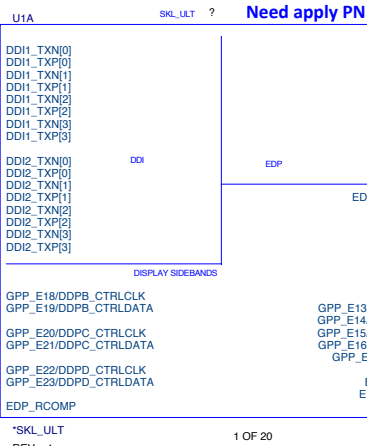
27 SDVO\_CLK  
27 SDVO\_DATA

TP2 1DDPC\_CTRLDATA

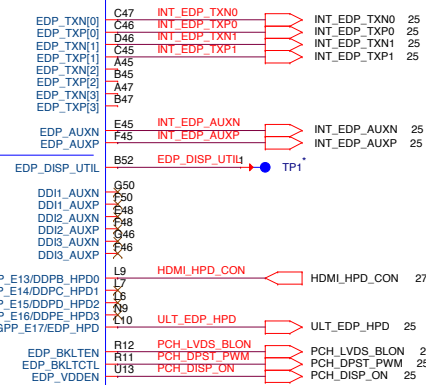
TP3 1DDPD\_CTRLDATA

+VCCIO R3 24.9\_1%\_4

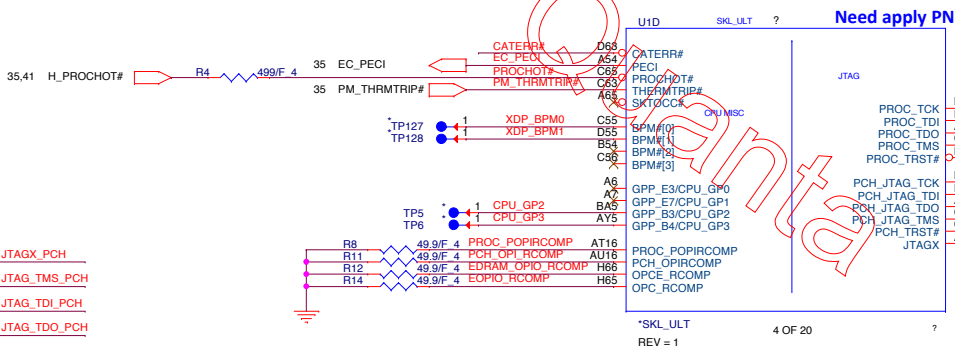
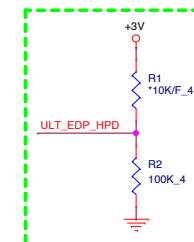
eDP\_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms



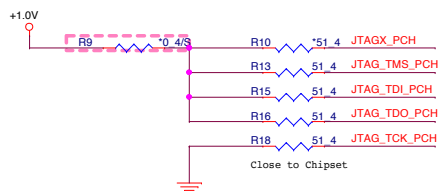
Justsurport FHD 1920x1080



Reserve EDP\_HPD opposites circuit!



+VCCSTPLL R6 49.9/F 4 CATERR#

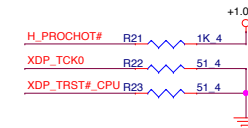


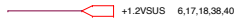
Close to EC

PM\_THRMTRIP# R5 1K\_4 +VCCSTPLL

Processor pull-up (CPU)  
TO BE REPLACED WITH 1K OHMS FOR SKL.  
470 OHM IS FOR I/P

PLACE NEAR CPU

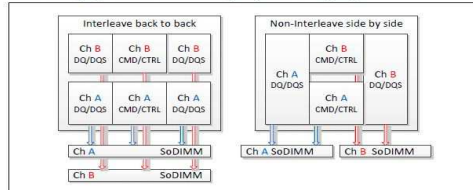




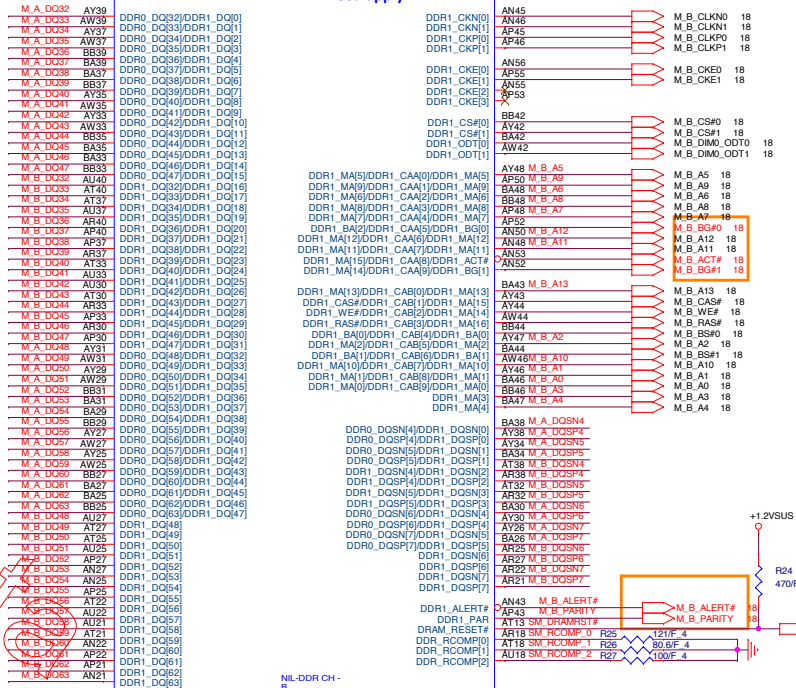
Need apply PN



### Interleave (IL) and Non-Interleave (NIL) Modes Mapping



Need apply PN



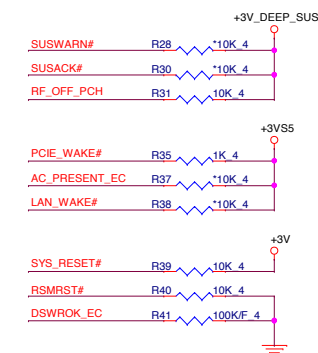
+1.2VSUS

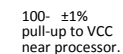
18  DDR3\_DRAMRST# 17,18

**PROJECT : NFLP\_KBLU\_DR**  
Quanta Computer Inc.




Size Custom	Document Number <b>03 – SKYLAKE 2/15(DDR4 I/F)</b>	Rev 1A
Date: Friday, March 24, 2017	Sheet 3 of 49	



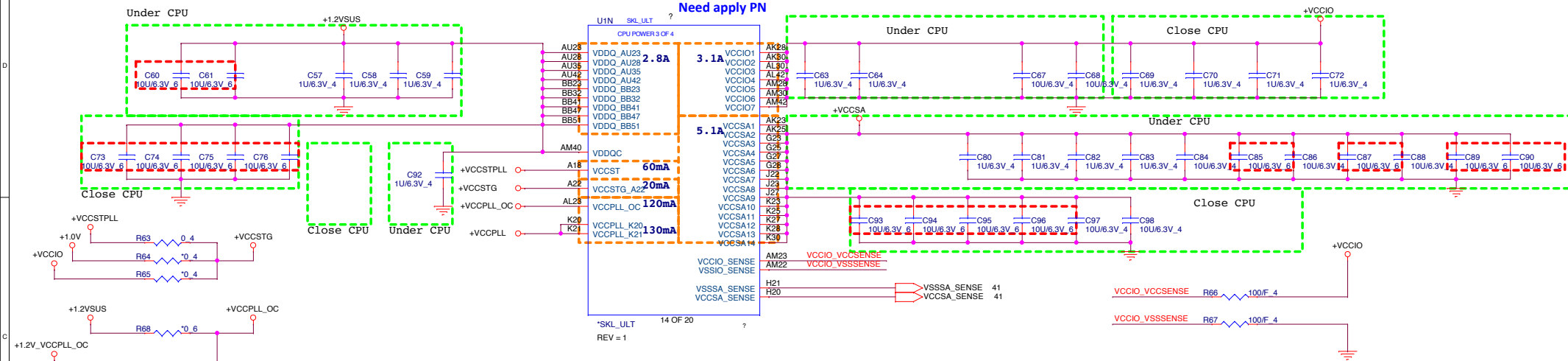


VR SVID DATA 41

	<b>PROJECT : NFLP_KBLU_DR</b> Quanta Computer Inc.		
	Size Custom	Document Number <b>05 -- SKYLAKE 4/15 (POWER-1)</b>	Rev 1A
Date: Friday, March 24, 2017		Sheet 5 of 49	

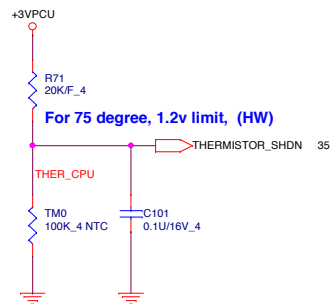
+VCCSTPLL 2,4,5,9,40,41  
 +VCCSA 41,43  
 +1.2VSUS 3,17,18,38,40  
 +1.0V\_DEEP\_SUS 9,13,15,39,40  
 +1.0V 2,4,35,40  
 +3VPCU 13,29,30,31,34,35,36,37,49

Need apply PN



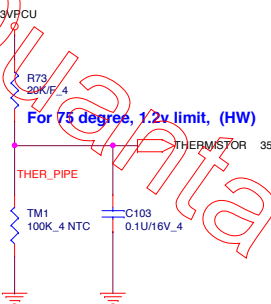
## IO Thrm Protect

For CPU USE



For 75 degree, 1.2v limit, (HW)

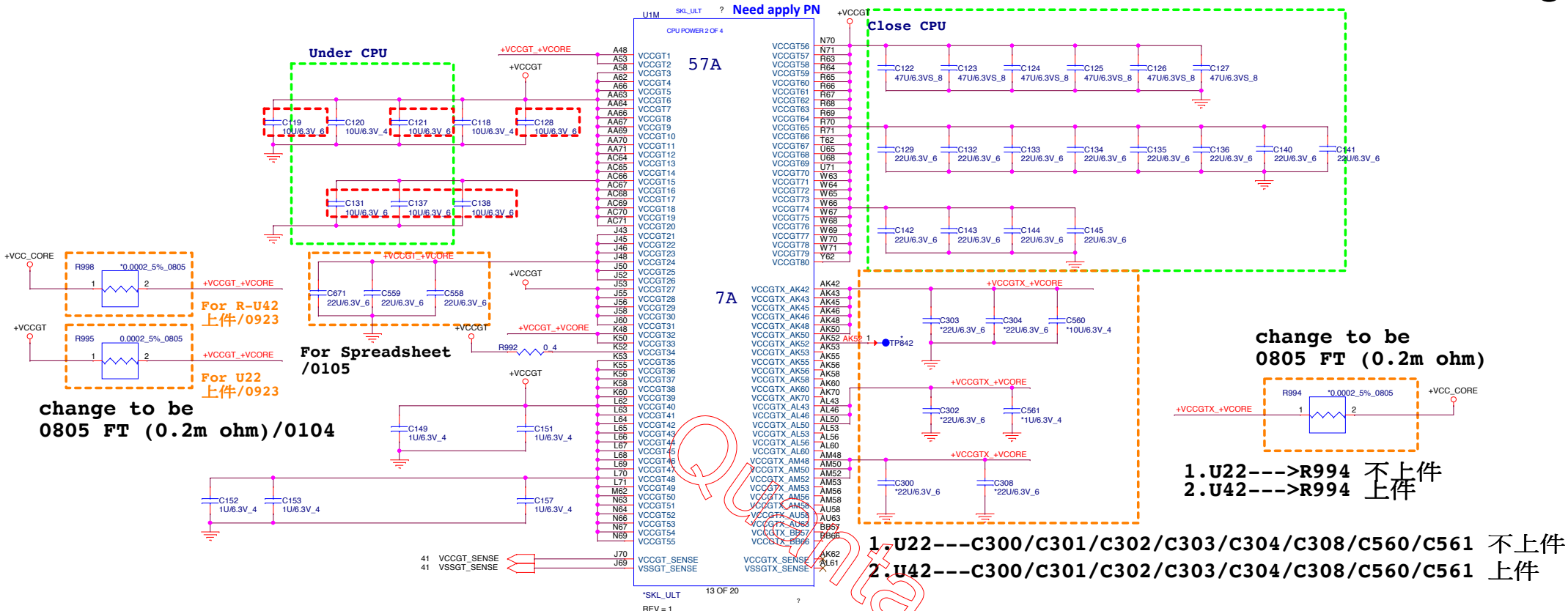
For PIPE USE



For 75 degree, 1.2v limit, (HW)

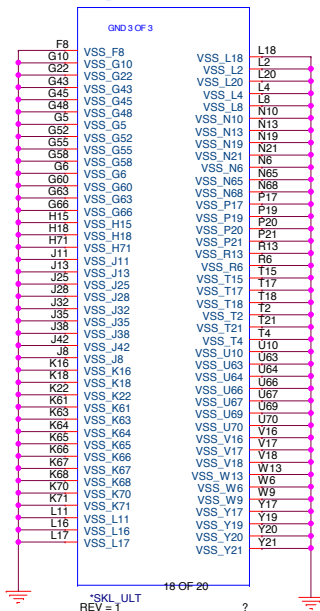
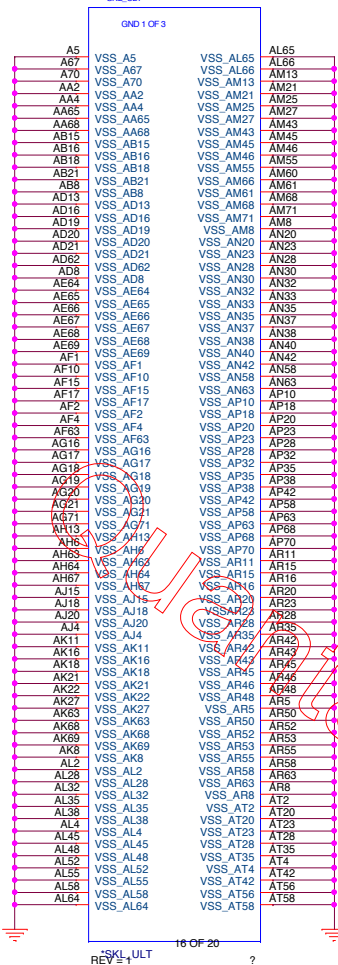
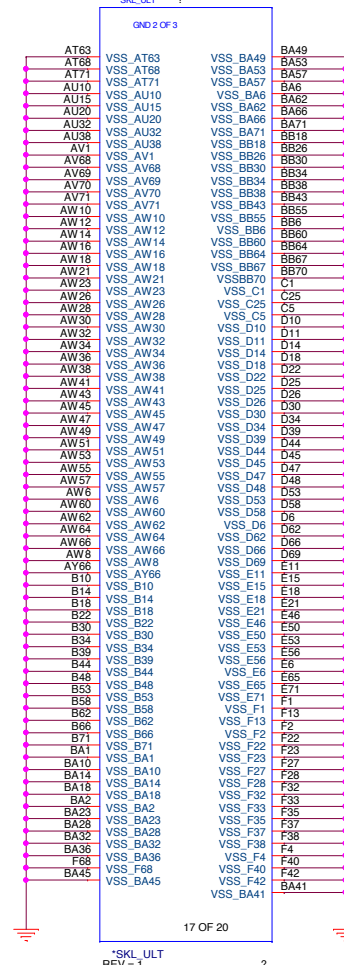
Power Rail	Description	Control
V <sub>CC</sub>	Processor IA Cores Power Rail	SVID
V <sub>CCGT</sub>	Processor Graphics Power Rails	SVID
V <sub>CCGTx</sub>	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V <sub>CCSA</sub>	System Agent Power Rail	SVID/Fixed (SKU dependent)
V <sub>CCIO</sub>	IO Power Rail	Fixed
V <sub>CCST</sub>	Sustain Power Rail	Fixed
V <sub>CCPLL</sub>	Processor PLLs power rail	Fixed
V <sub>DDQ</sub>	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V <sub>CCOPC</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCOPC_1P8</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CC_EOPIO</sub>	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

+VCCGT 41,43  
+VCC\_CORE 5,41,42  
+1.2VSUS 3,6,17,18,38,40

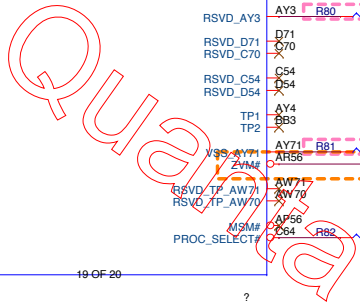


Power Rail	Description	Control
V <sub>CC</sub>	Processor IA Cores Power Rail	SVID
V <sub>CCGT</sub>	Processor Graphics Power Rails	SVID
V <sub>CCGTx</sub>	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V <sub>CCSA</sub>	System Agent Power Rail	SVID/Fixed (SKU dependent)
V <sub>CCIO</sub>	IO Power Rail	Fixed
V <sub>CCST</sub>	Sustain Power Rail	Fixed
V <sub>CCPLL</sub>	Processor PLLs power rail	Fixed
V <sub>DDQ</sub>	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V <sub>CCOPC</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCOPC_1P8</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCEOPIO</sub>	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed



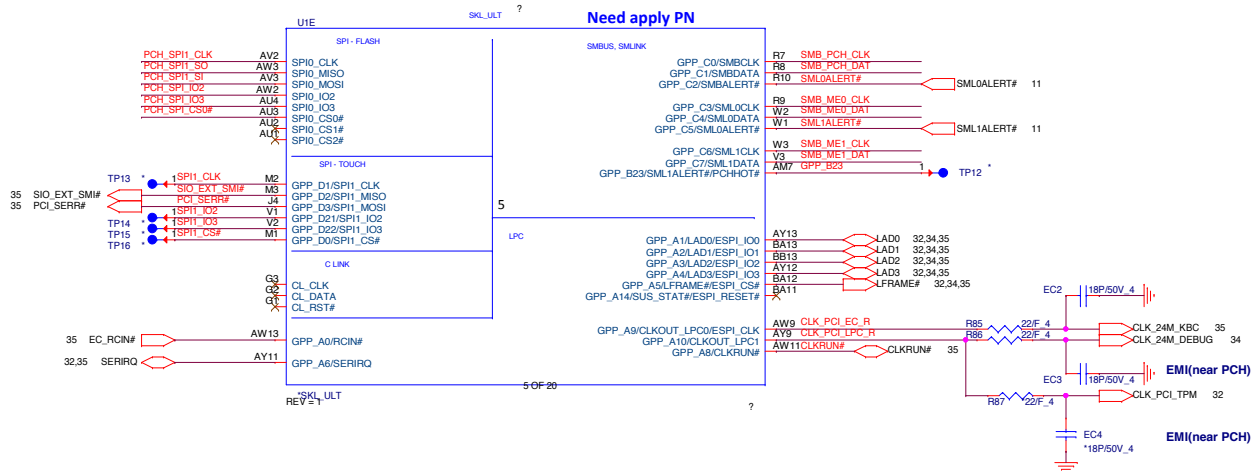
U1R  
SKL\_ULT ? Need apply PNU1P  
SKL\_ULT ? Need apply PNU1Q  
SKL\_ULT ? Need apply PN



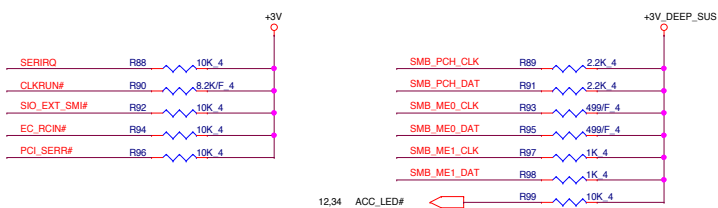


	1	0	Circuit
CFG3 (Physical Debug Enable) DFX_Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSF	
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	

+3V\_DEEP\_SUS 4,11,12,14,15,18  
 +3V 2,4,11,12,13,14,15,17,18,25,26,27,28,29,31,32,33,34,35,41,48  
 +5V 25,26,27,31,32,34,48,50  
 +1.0V 2,4,6,35,40  
 +3VSS 4,15,25,34,35,37,38,39,40,44,47,48,50



## GPIO Pull UP



## PCH SPI ROM(CLG)

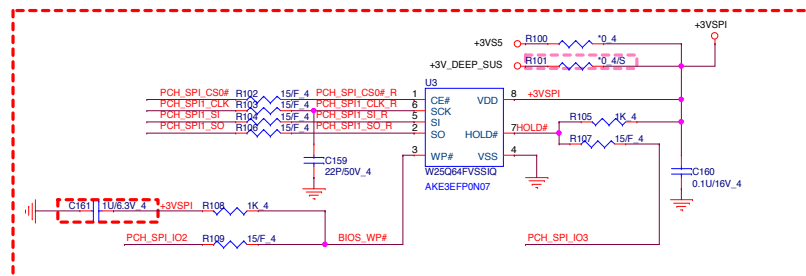
Vender	Size	P/N
EON	8MB	AKE3EZN0Q01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFHS08FS023

35 PCH\_SPI\_CS0# R  
 35 PCH\_SPI\_CLK R  
 35 PCH\_SPI\_SI R  
 35 PCH\_SPI\_SO R

need place to TOP

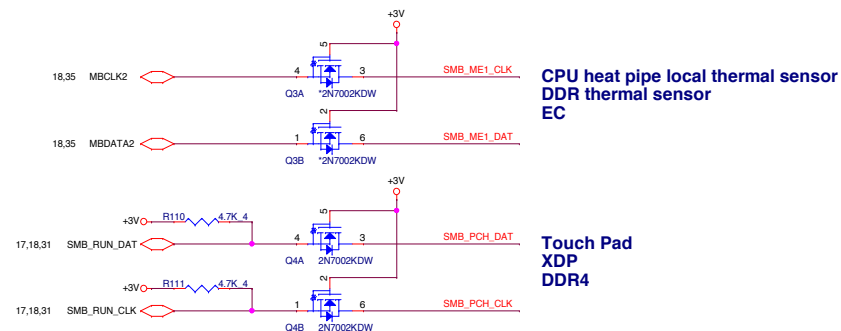
TP17 1 PCH\_SPI\_CS0# R  
 TP18 1 PCH\_SPI\_CLK R  
 TP19 1 PCH\_SPI\_SI R  
 TP20 1 PCH\_SPI\_SO R  
 TP21 1 BIOS\_WP#  
 TP22 1 HOLD#

## PCH SPI ROM(CLG)



1005 Change P/N to DFHS08FS023(Socket)

## SMBus/Pull-up(CLG)

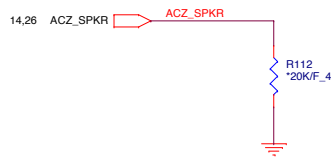


PROJECT : NFLP\_KBLU\_DR  
Quanta Computer Inc.

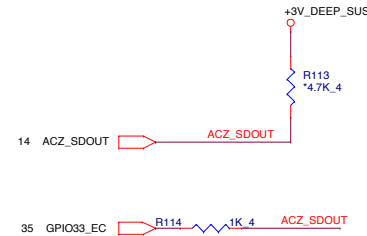
Size Custom Document Number 10 -- SKYLAKE 09/15(SPI/LPC/SM) Rev 1A  
 Date: Friday, March 24, 2017 Sheet 10 of 49

# Functional Strap Definitions

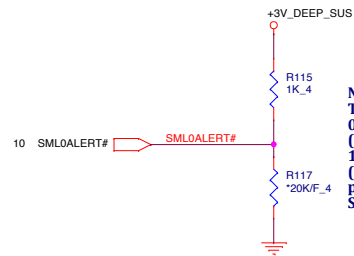
**DESIGN NOTE:**  
**WEAK PULL UP RESISTOR PRESENT ON THIS NET**



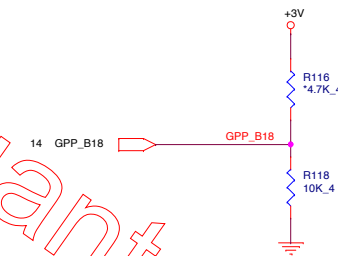
**TOP SWAP OVERRIDE**  
**HIGH - TOP SWAP ENABLE**  
**LOW-DISABLED**  
**HIGH: LPC SELECTED FOR SYSTEM FLASH**  
**WEAK INTERNAL PD**



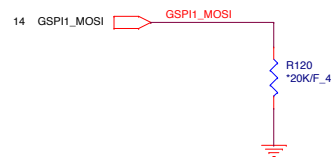
**No Boot:**  
The signal has a weak internal pull-down.  
0 = Enable security measures defined in the Flash Descriptor.  
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.



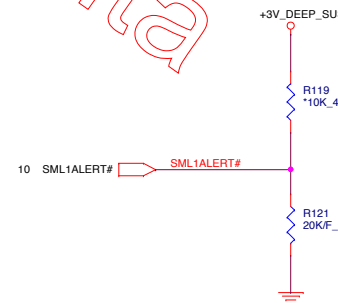
**No Boot:**  
The signal has a weak internal pull-down.  
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).  
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.



**No Boot:**  
The signal has a weak internal pull-down.  
0 = Disable No Reboot mode.  
1 = Enable No Reboot mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.



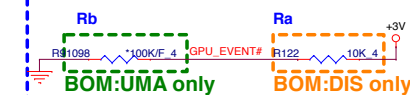
**No Boot:**  
The signal has a weak internal pull-down.  
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.  
**Bit 10      Boot BIOS Destination**  
0            SPI  
1            LPC



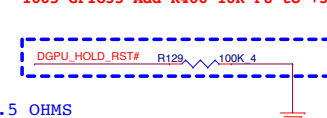
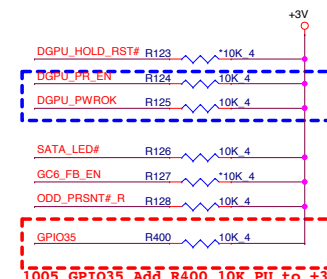
**No Boot:**  
The signal has a weak internal pull-down.  
0 = LPC is selected for EC.  
1 = eSPI is selected for EC.

Need apply PN

GFX Present



	SG(Default)	UMA
Stuff	Ra	Rb
NC	Rb	Ra



If OTG is not implemented on the platform, then USB2\_ID and USB2\_VBUSSENSE should both be connected to ground.

GPIO35:  
SSD SATA IF => High  
SSD PCIE IF => Low

USB3.0 Small Board  
DB 1SPD 9/29USB3.0 Small Board  
DB 1SPD 9/292017/9/29  
To USB3 Type C2017/9/29  
To USB3 Type CUSB3.0 Small Board  
DB 1SPD 9/29

Combo USB3.0 Small Board

Camera

Type C 9/29

IR CAM

for Cardreader IC 9/29

WLAN

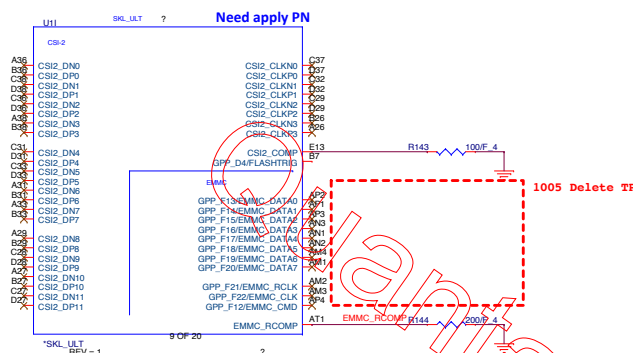
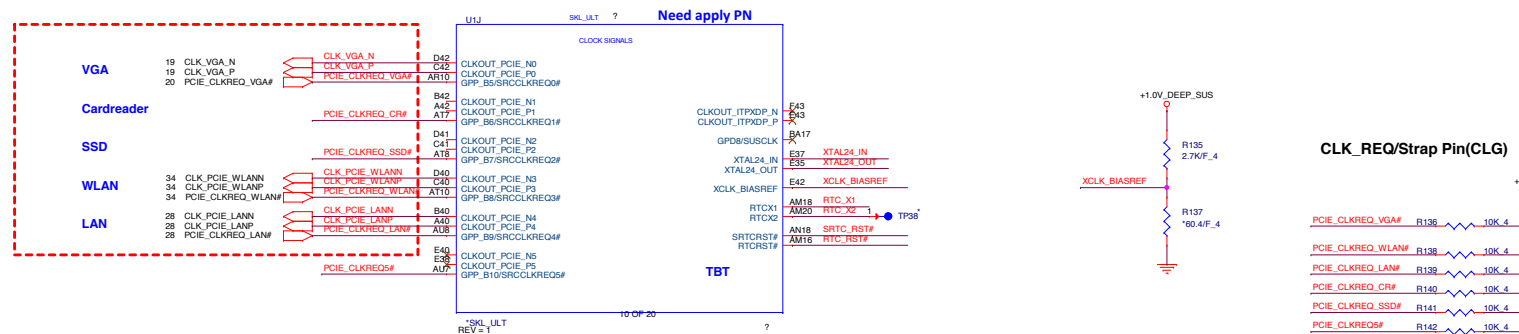
Touch Screen

PLACE 'Ra' WITHIN 500 MILS  
FROM USB2\_COMP PIN WITH  
TRACE IMPEDANCE LESS THAN 0.5 OHMS

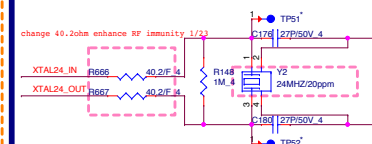
Need apply PN

SSIC / USB3

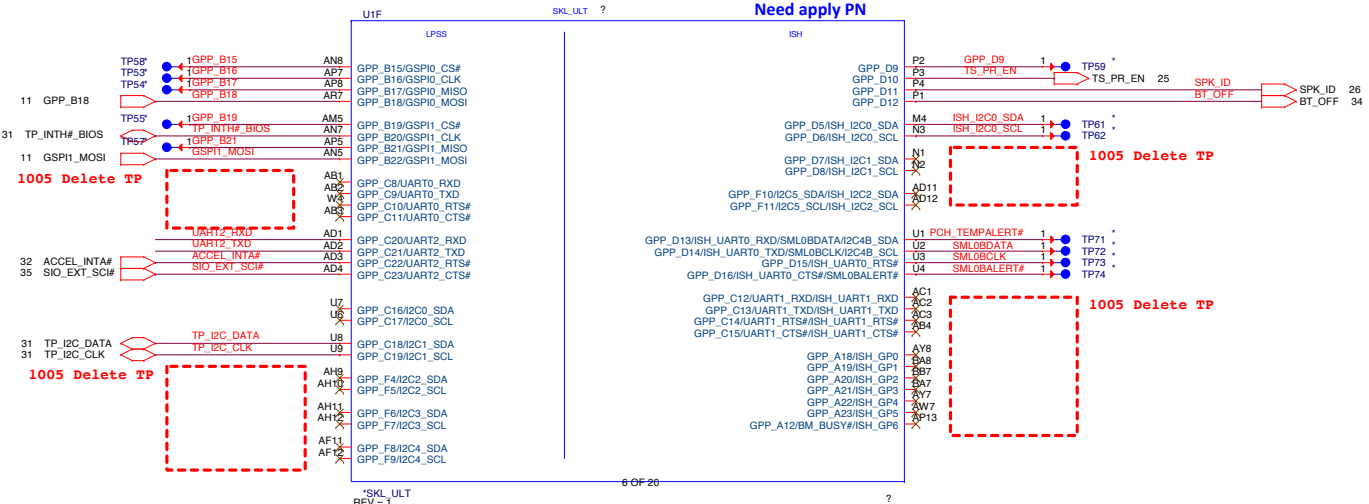
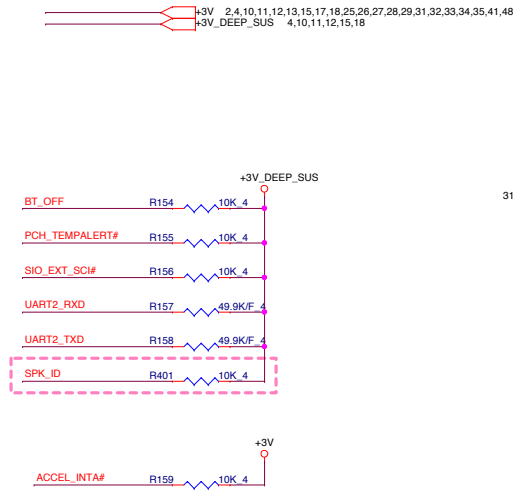
USB3\_1\_RXN  
USB3\_1\_RXP  
USB3\_1\_TXN  
USB3\_1\_TXPUSB3\_2\_RXN/SSIC\_1\_RXN  
USB3\_2\_RXP/SSIC\_1\_RXP  
USB3\_2\_TXN/SSIC\_1\_TXN  
USB3\_2\_TXP/SSIC\_1\_TXPUSB3\_3\_RXN/SSIC\_2\_RXN  
USB3\_3\_RXP/SSIC\_2\_RXP  
USB3\_3\_TXN/SSIC\_2\_TXN  
USB3\_3\_TXP/SSIC\_2\_TXPUSB3\_4\_RXN  
USB3\_4\_RXP  
USB3\_4\_TXN  
USB3\_4\_TXPUSB2N\_1  
USB2P\_1USB2N\_2  
USB2P\_2USB2N\_3  
USB2P\_3USB2N\_4  
USB2P\_4USB2N\_5  
USB2P\_5USB2N\_6  
USB2P\_6USB2N\_7  
USB2P\_7USB2N\_8  
USB2P\_8USB2N\_9  
USB2P\_9USB2N\_10  
USB2P\_10USB2N\_11  
USB2P\_11USB2N\_12  
USB2P\_12USB2N\_13  
USB2P\_13USB2N\_14  
USB2P\_14USB2N\_15  
USB2P\_15USB2N\_16  
USB2P\_16USB2N\_17  
USB2P\_17USB2N\_18  
USB2P\_18USB2N\_19  
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USB2P\_158USB2N\_159  
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USB2P\_231



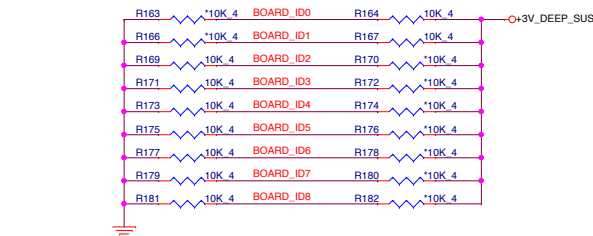
The 24 MHz (50 Ohm ESR) XTAL used for Skylake-U needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-U.



## Skylake (GPIO)

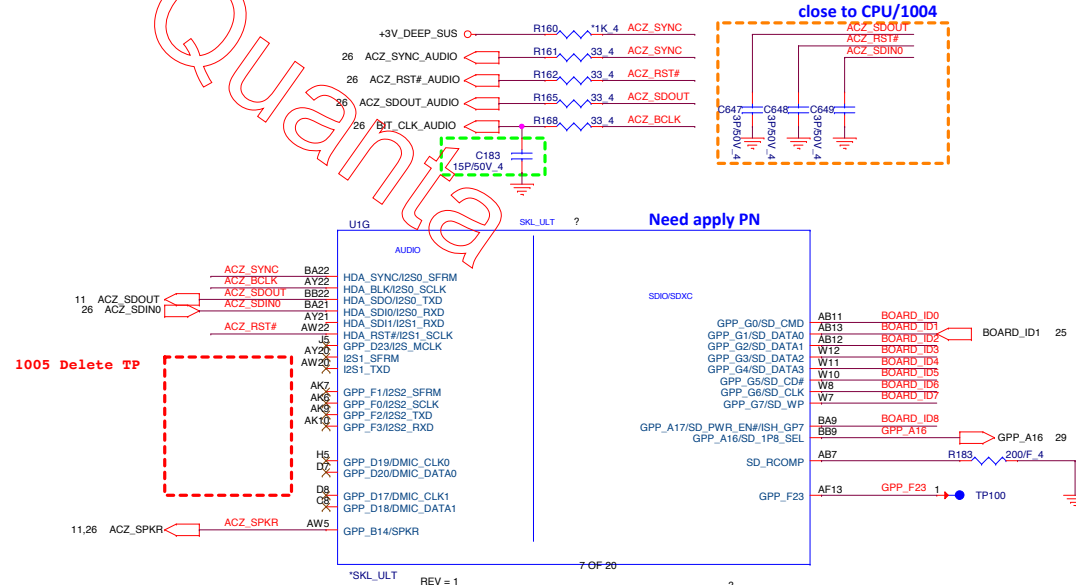


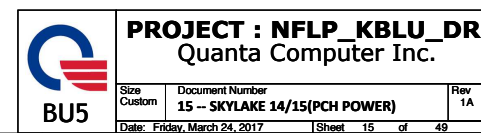
## HDA Bus(CLG)



Skylake	BOARD_ID[8:5]	BOARD_ID[5]	Board ID 4	Board ID 3	BOARD_ID[2:1]	BOARD_ID0
Model	ID8 ID7 ID6	ID5	ID4	ID3	ID2 ID1	ID0
Definition	Reserve (Default = 000)	GPU 0 : AMD 1 : Intel	0 4 VRAMs 1 8 VRAMs	0 VGA CAM 1 IR CAM	01 14" (14" cable is 00) 01 15" 1SPD 10 17" 11 2SPD	0 : UMA 1 : DIS


ID1(R167)always 上件

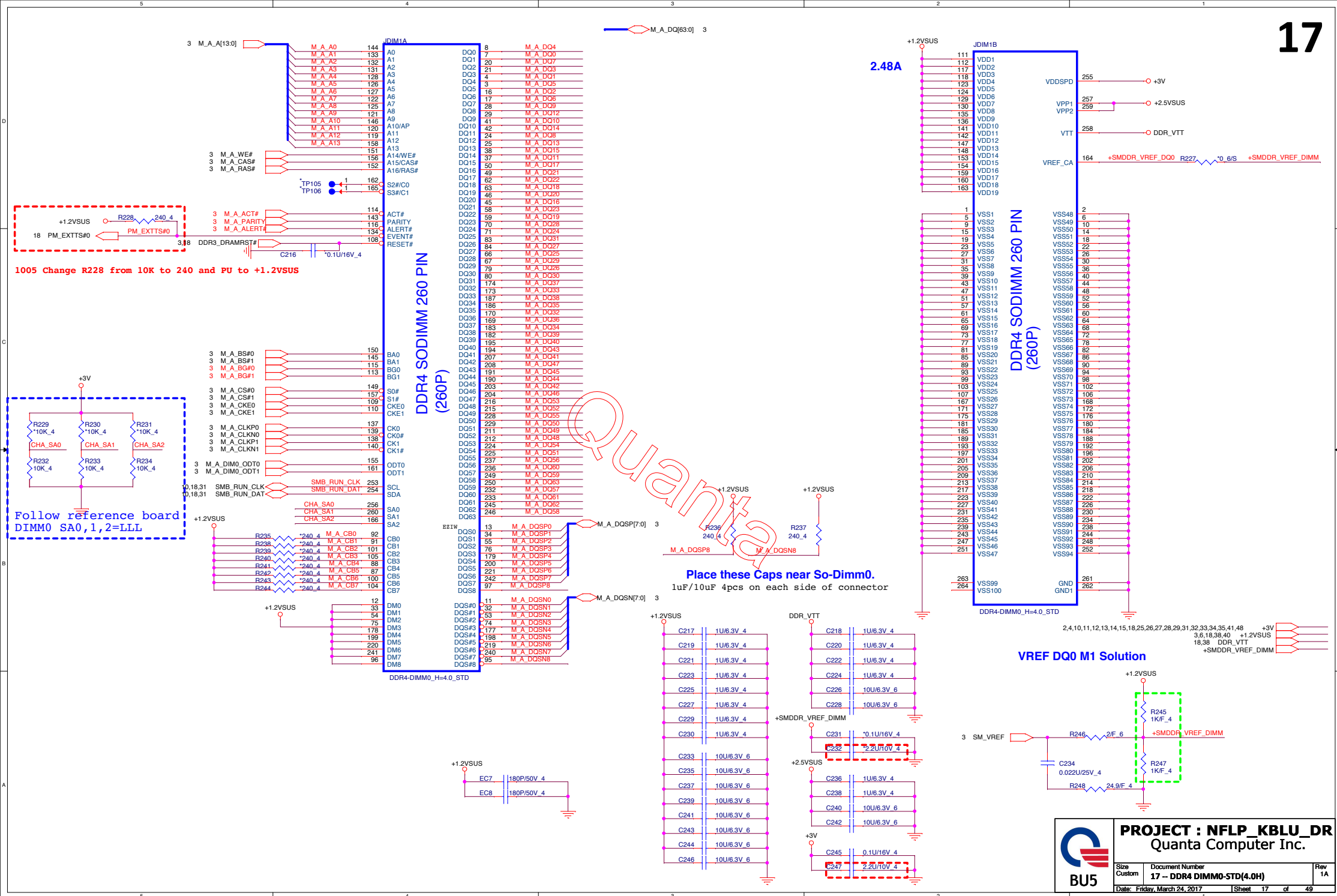


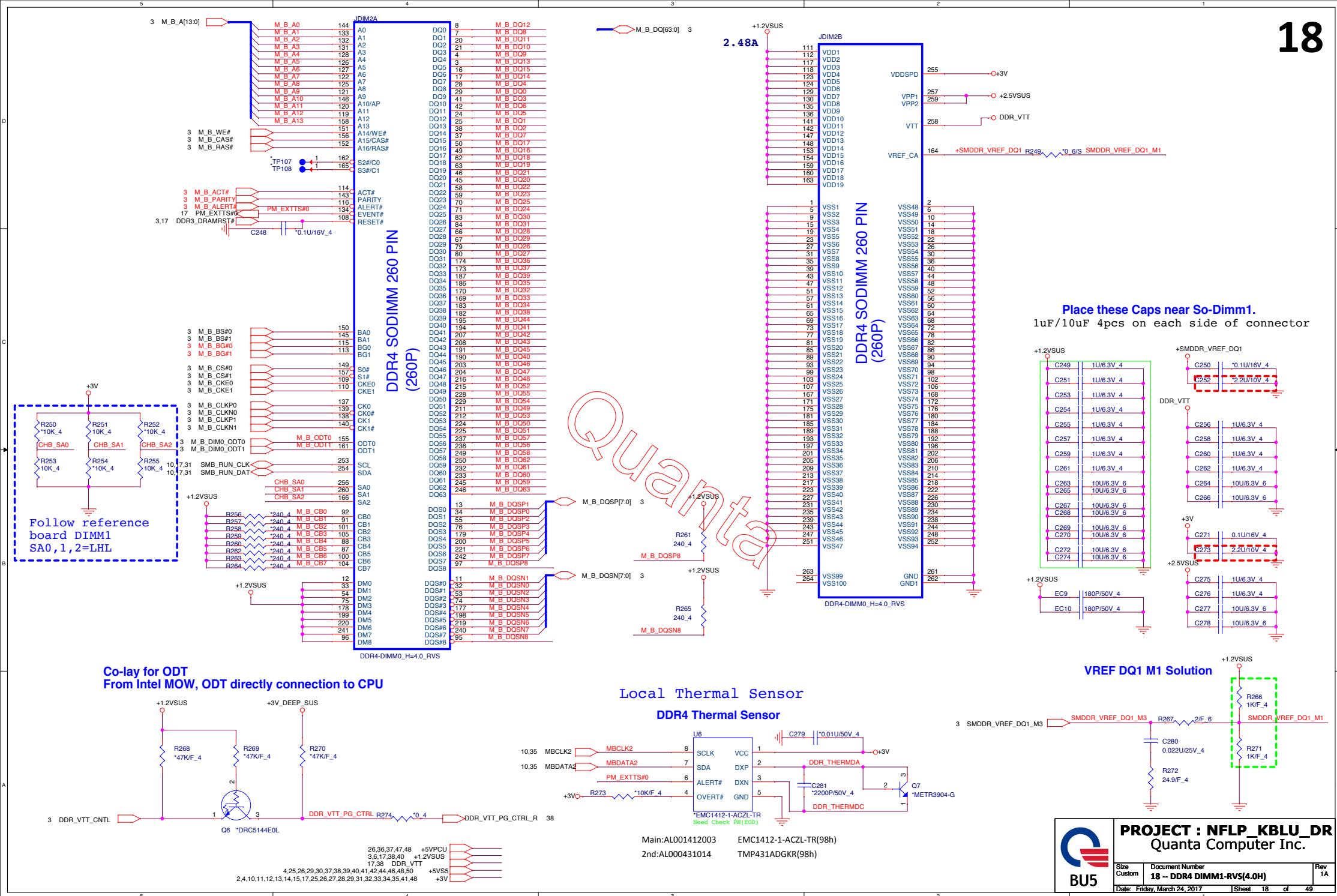


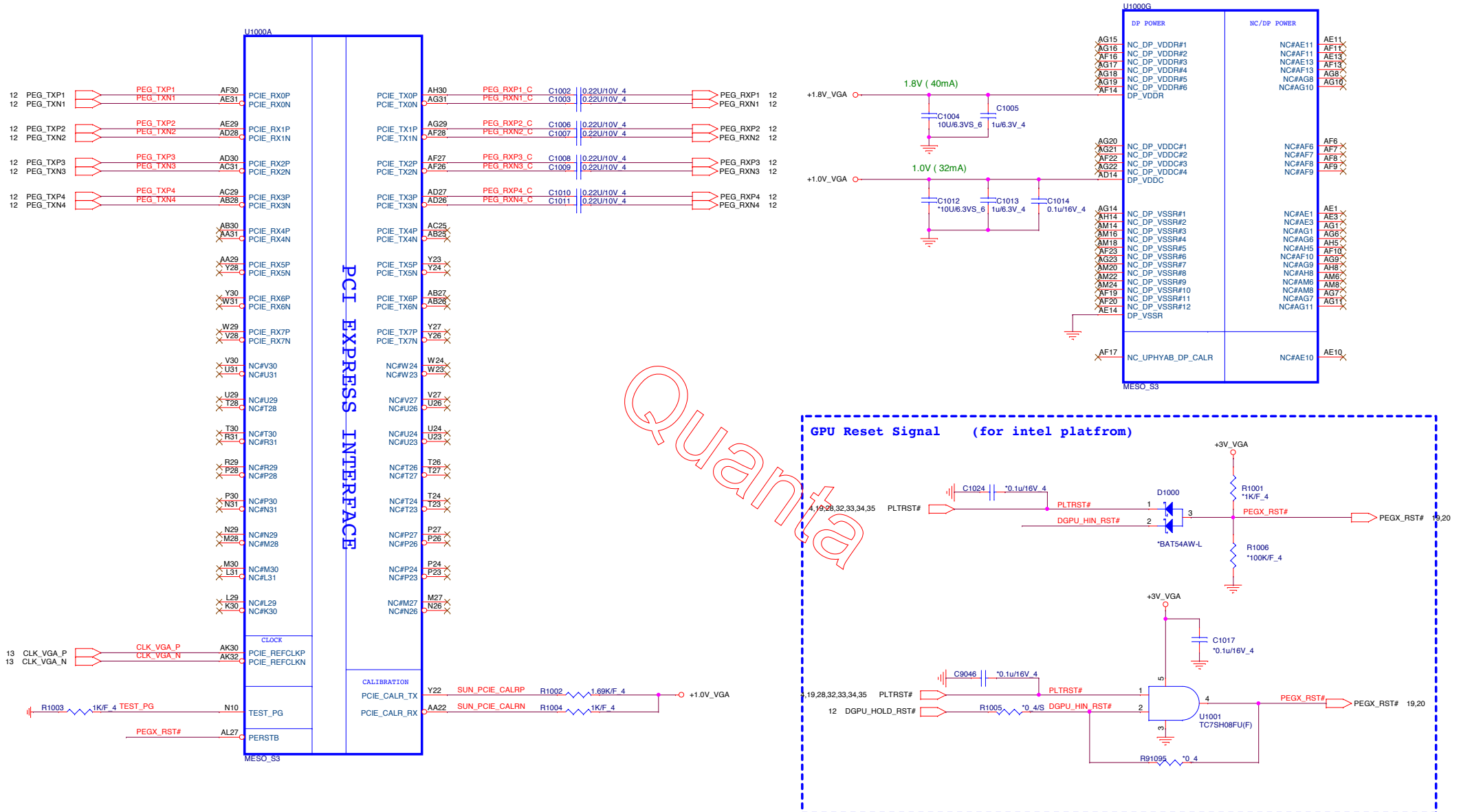


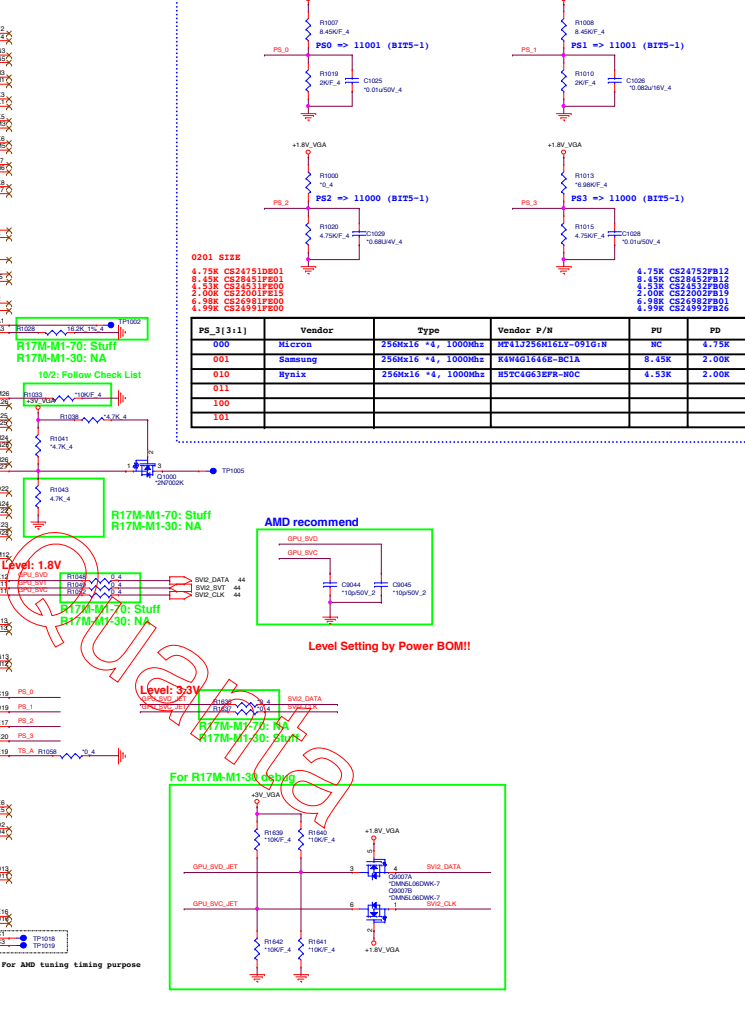
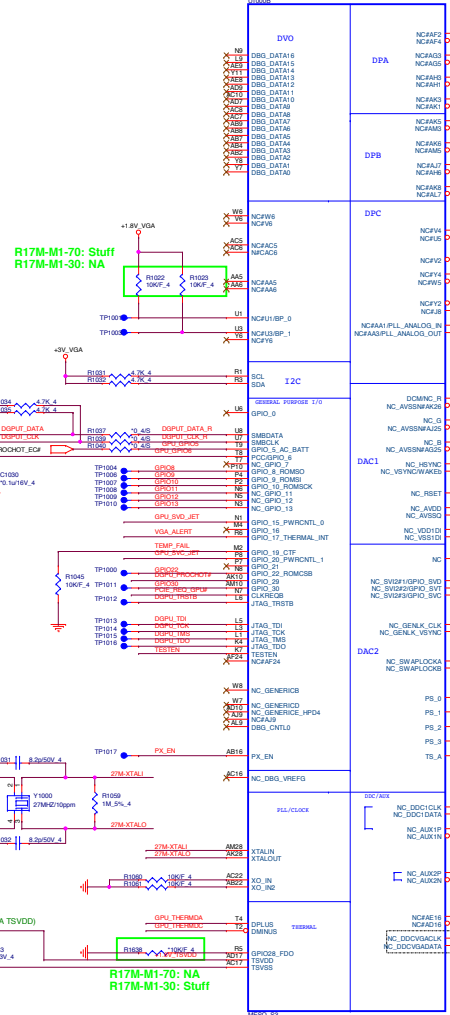
Quanta

 <b>BU5</b>	<b>PROJECT : NFLP_KBLU_DR</b> Quanta Computer Inc.		
	Size	Document Number	Rev
		<b>16 -- SKYLAKE 15/15 XDP&amp;APS *</b>	<b>1A</b>
Date: Friday, March 24, 2017		Sheet	16 of 49









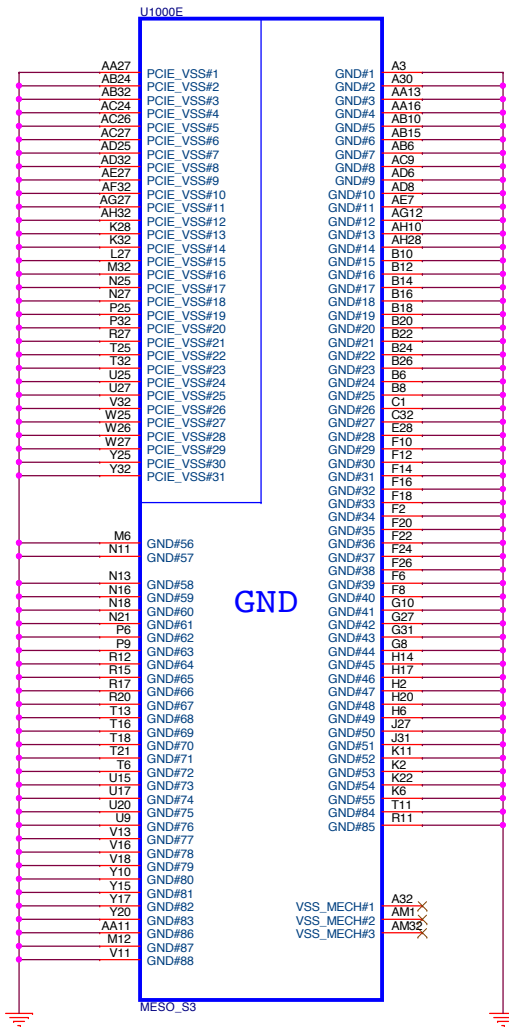
<b>MPS Implementation</b>			
Connect GPIO_28 to I/O pin provided to enable MPS			
Many of PS, CIO[2-3] not used, leave "no connect"			
C may be PS, CIO[2-3] or not, must be correctly populated per tables below			
All components are 1% tolerance, except for the ADC is 0.1% tolerance			
Total DC resistance of trace between PS-gm and C should be less than 2 ohms			
Total DC resistance of trace between C and R should be less than 2 ohms			
Trace capacitance should be less than 100pf. Resistor should be +/-1% tolerance			

Capacitor Location	Resistor Device	Lookup Table
C (W/F)	BIBS(A)	R <sub>ps</sub> (Ohm)    R <sub>gm</sub> (Ohm)    B(CIO,3,1)
680    00	NC	4750    000
82     01	NC	2000    001
10     10	4530	4530    010
NC     11	6980	4990    011
	4530	4990    100
	3240	5620    101
	2040	10000    102
	20K	4750     110

Size of the Primary Memory Apertures	ROM_CONFIG[2:0]
128 MB	000
256 MB	001
64 MB	010
Reserved	011
512 MB	Not Supported
1 GB	Not Supported
2 GB	Not Supported
4 GB	Not Supported

MLPS bit	Strap Name	Description	Recommended settings
PS_0101	ROM_CONFIG01	If STRAP_BIOS_ROM_EN = 1, ROM_CONFIG01 defines the ROM type.	Design dependent, see the Description.
PS_0102	ROM_CONFIG01	If STRAP_BIOS_ROM_EN = 0, ROM_CONFIG01 defines the primary security aperture size. See Security Hardware Aperture Size (p. 25).	
PS_0104	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_1111	STRAP_BIF_GEN1_EN	PCIE GEN1 capability. • 1 = PCIE GEN1 is supported. • 0 = PCIE GEN1 is not supported. Determine whether or not the PCIE reference clock power management capability is reported in the PCI configuration space via the bit in the CLACKR power management capability is disabled.	Design dependent, see the Description.
PS_1121	STRAP_BIF_CLK_PN_EN	• 0 = The CLACKR power management capability is disabled. • 1 = The CLACKR power management capability is enabled.	0
PS_1123	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1141	STRAP_TX_CTL_PULV_SWING	Control the transmitter full-swing mode. • 0 = The transmitter full-swing is enabled. • 1 = The transmitter full-swing is disabled.	1
PS_1121	STRAP_TX_DEEMPH_EN	PCI EXPRESS transmitter, de-emphasis enable. • 0 = Tx deemphasis disabled. • 1 = Tx deemphasis enabled.	Design dependent, see the Description.
PS_1122	N/A	Reserved.	0
PS_1122	N/A	Reserved.	0
PS_2121	STRAP_BIOS_ROM_EN	To enable the external BIOS ROM device. • 0 = Enable the external BIOS ROM device. • 1 = Enable the external BIOS ROM device.	Design dependent, see the Description.
PS_2140	N/A	Reserved.	1
PS_2141	N/A	Reserved.	1
PS_3121	BOARD_CONFIG01	Board configuration related information, such as for memory ID.	Design dependent, see the Description.
PS_3122	BOARD_CONFIG01	Reserved.	1
PS_3140	N/A	Reserved.	1
PS_3141	N/A	Reserved.	1



# CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS  
0= DO NOT INSTALL RESISTOR  
1 = INSTALL 3K RESISTOR  
X = DESIGN DEPENDANT  
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSNC	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

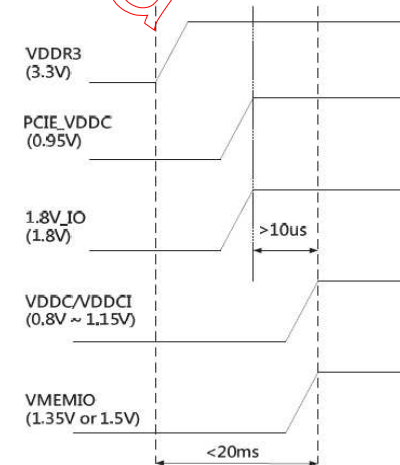
## NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

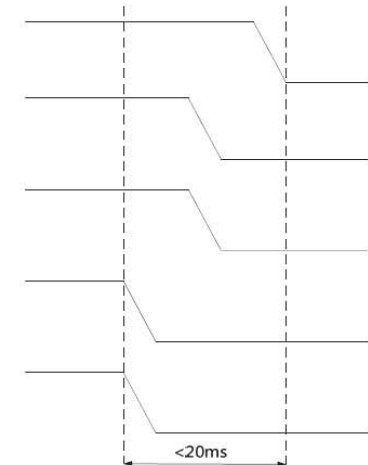
GPIO21 H2SYNC GENERICC GPIO8 GPIO2

## POWER UP / POWER DOWN SEQUENCE

### POWER UP

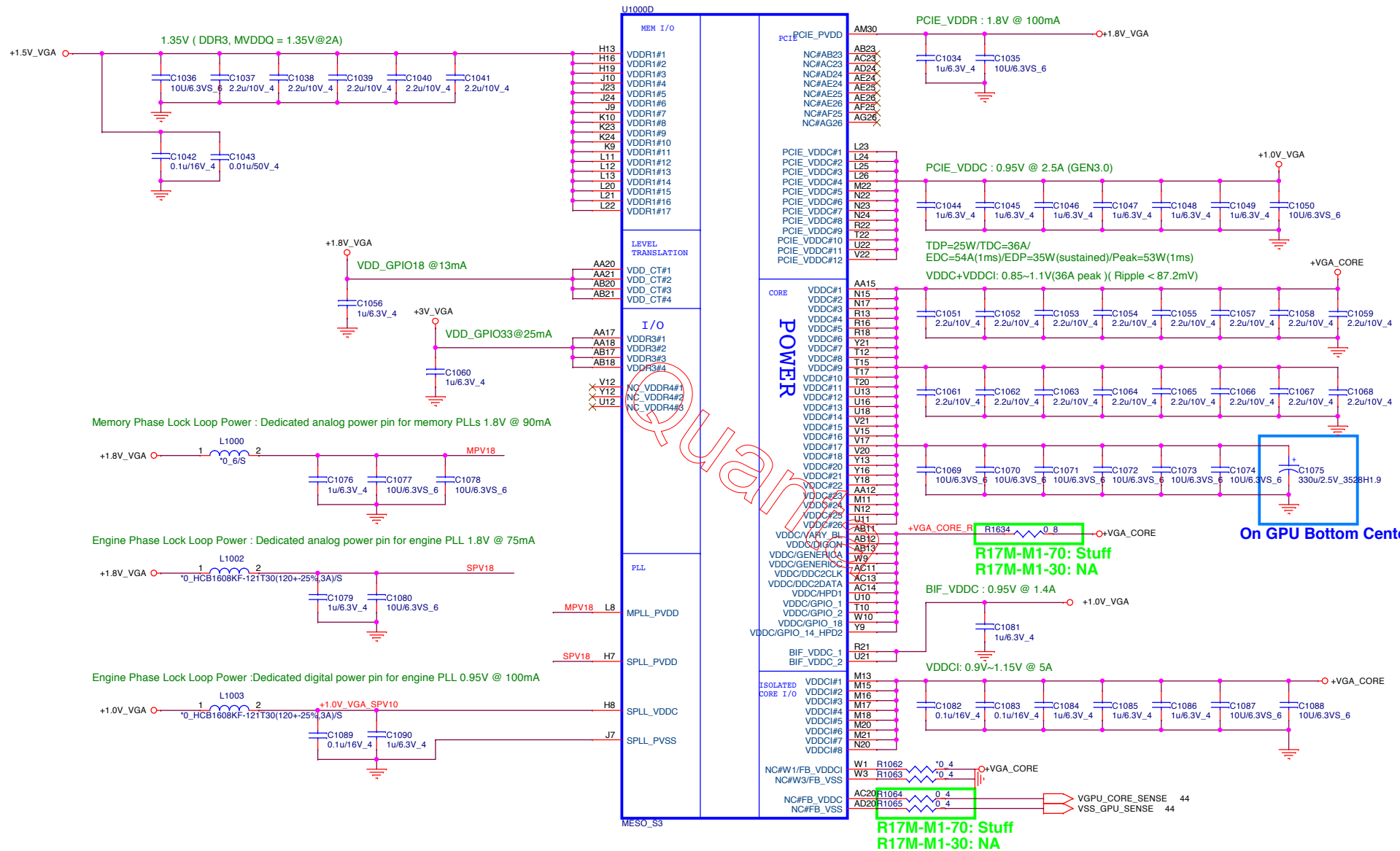


### POWER DOWN



**PROJECT : G54A**  
Quanta Computer Inc.

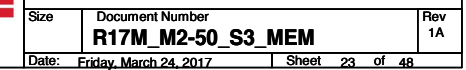
Size	Document Number	Rev
	<b>R17M_M2-50_DIS/GND</b>	1A
Date:	Friday, March 24, 2017	Sheet 21 of 48



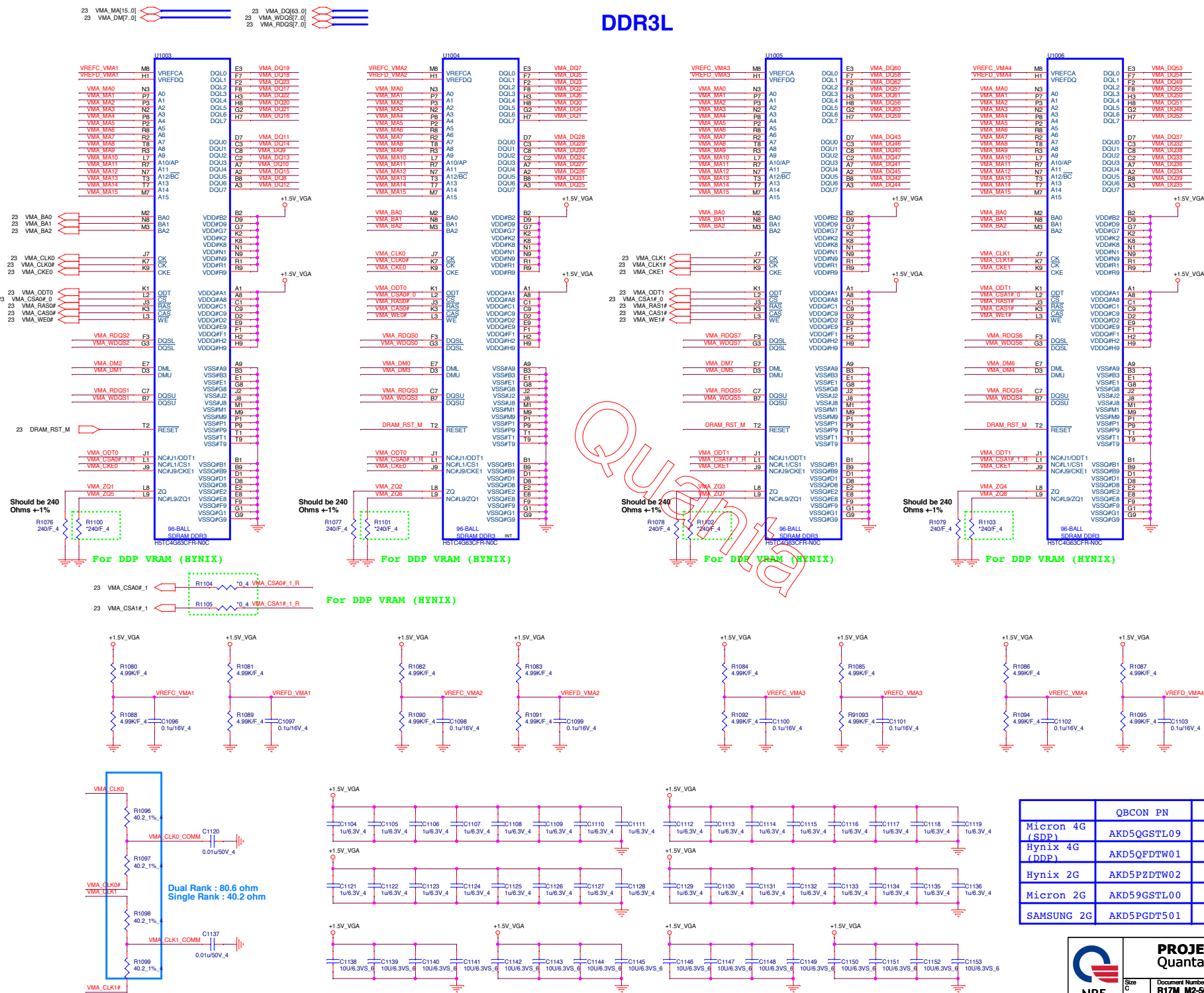
**PROJECT : G54A**  
Quanta Computer Inc.

Size	Document Number	Rev
	<b>R17M_M2-50_S3_POWER</b>	1A
Date:	Friday, March 24, 2017	Sheet 22 of 48



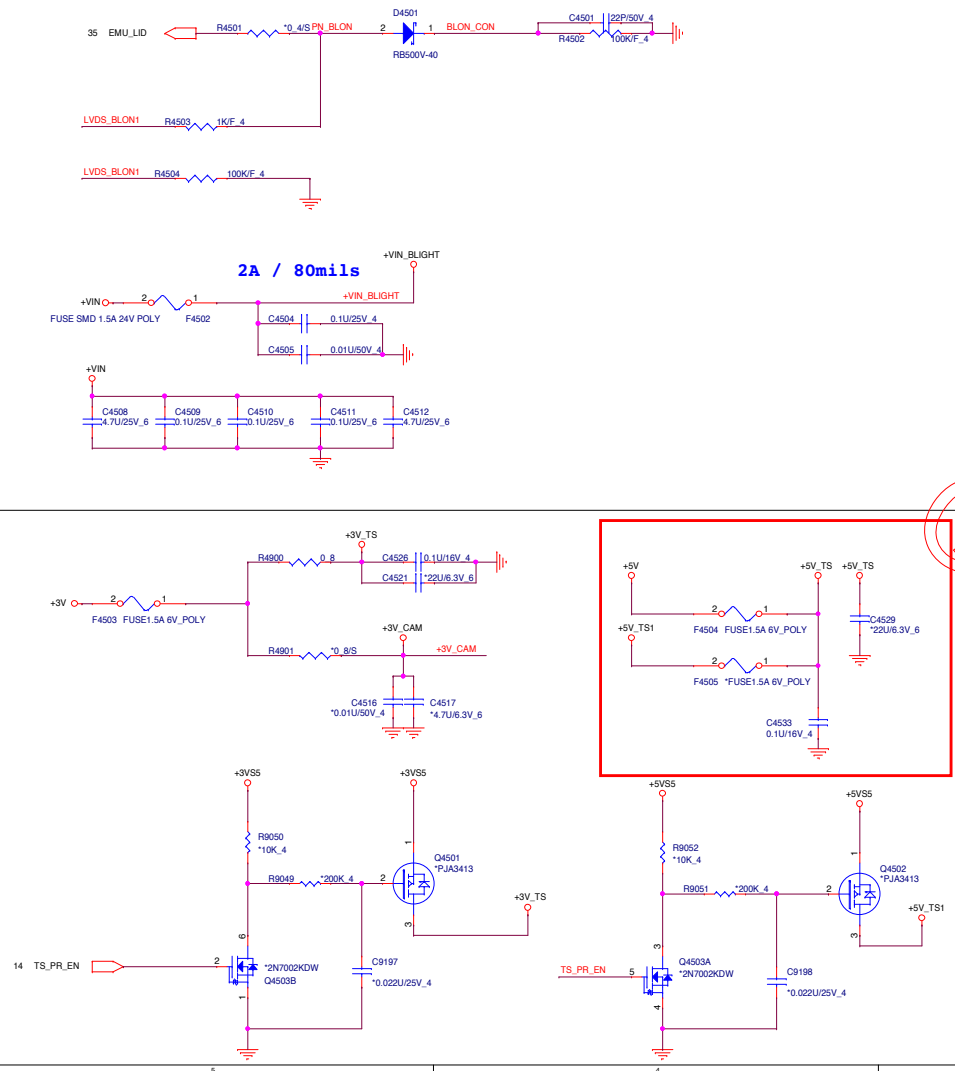


## DDR3L

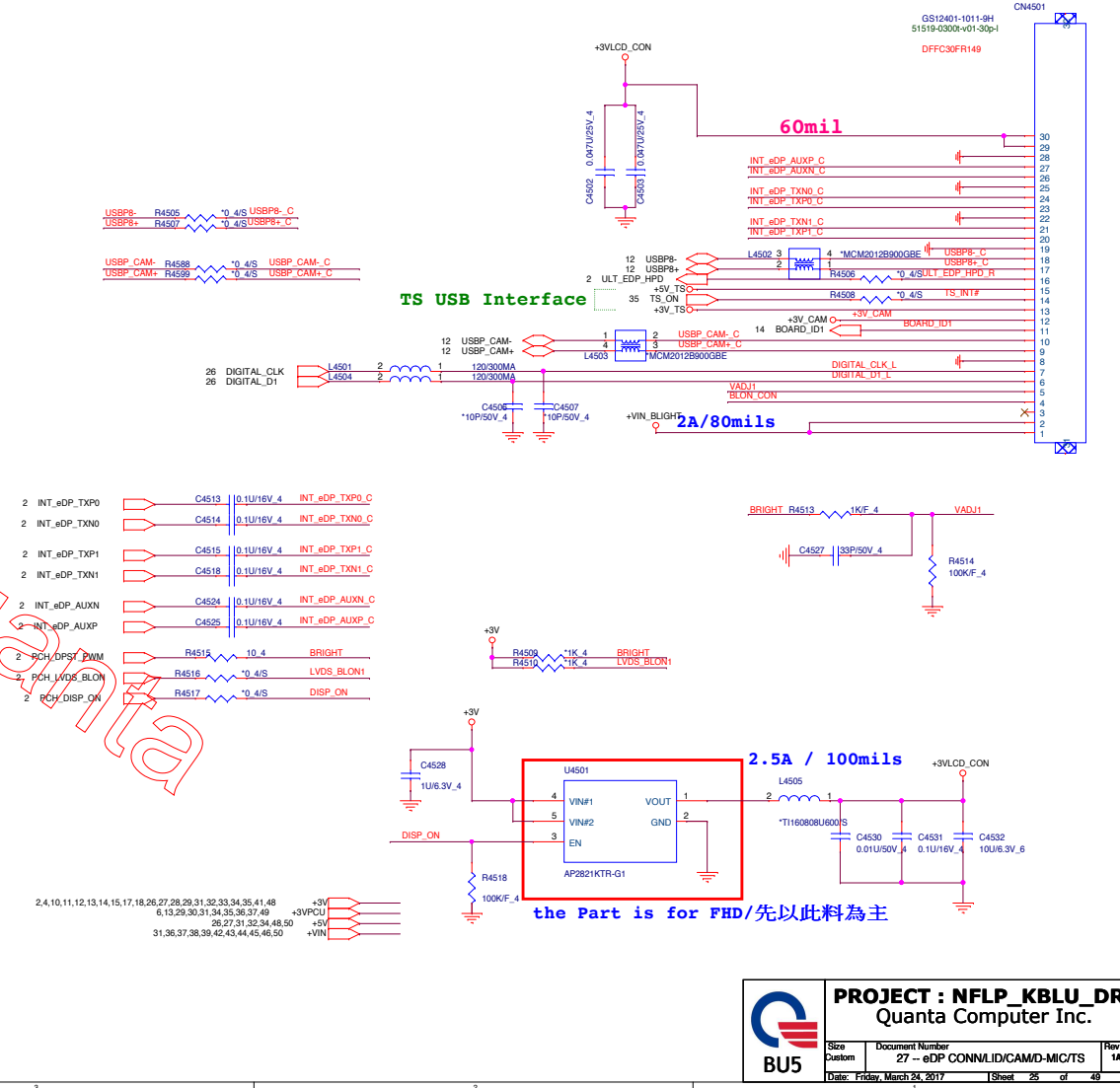


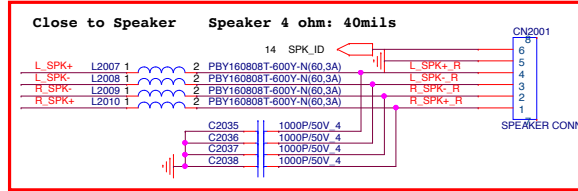
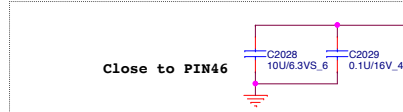
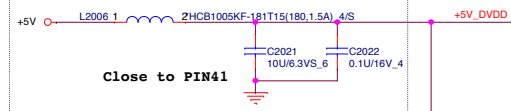
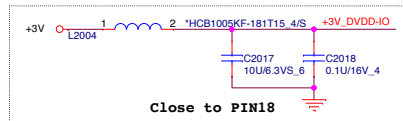
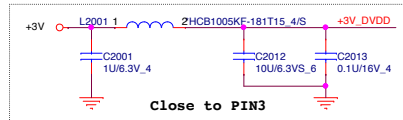
	QBCON PN	TOP BSQ
Micron 4G (SDP)	AKD5QGSTL09	AKD5QGSTL05
Hynix 4G (DDP)	AKD5QFDTW01	AKD5QFDTW00
Hynix 2G	AKD5PZDTW02	AKD5PZDTW01
Micron 2G	AKD59GSTL00	AKD59GSTL01
SAMSUNG 2G	AKD5PGDT501	AKD5PGDT500

# LID Switch

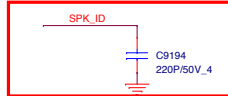


# eDP Conn.

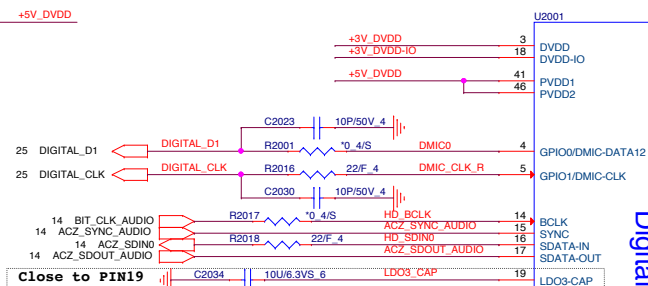




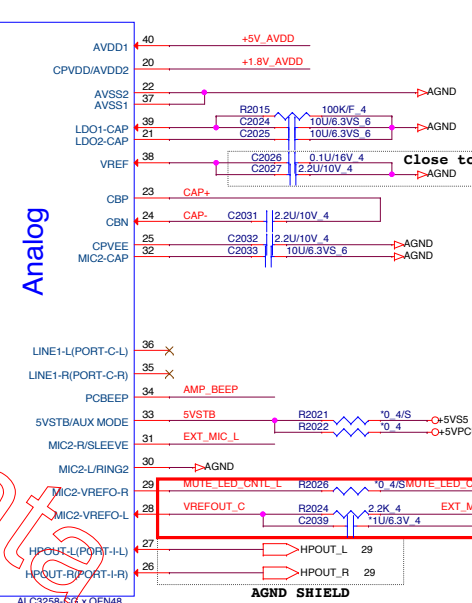
SPK\_ID for Smart amp feature



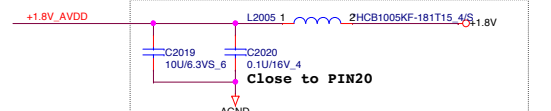
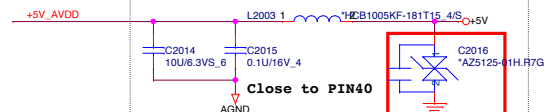
EMI suggestion 0119



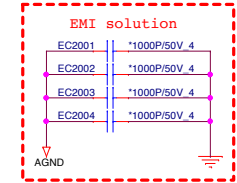
Analog



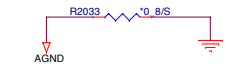
+5V\_AVDD &gt;40mils trace change PN to BC512501Z00 1/23



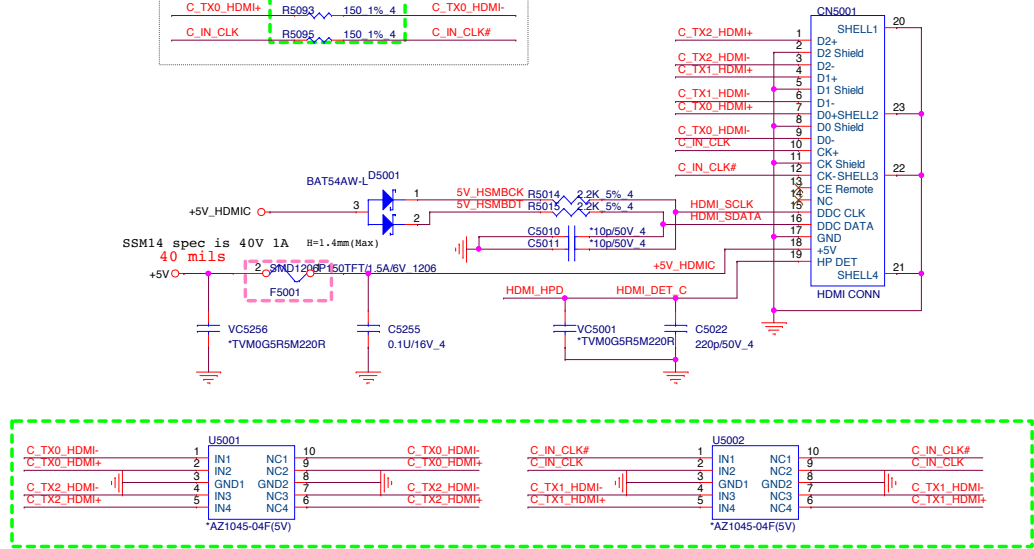
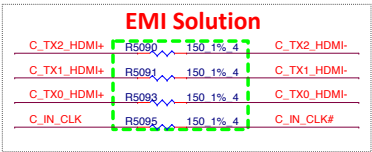
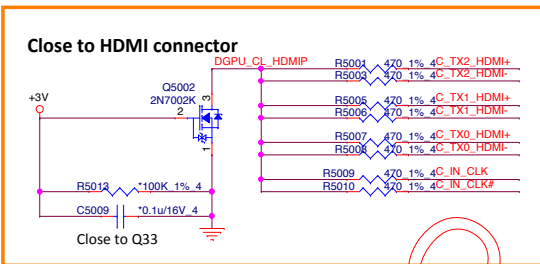
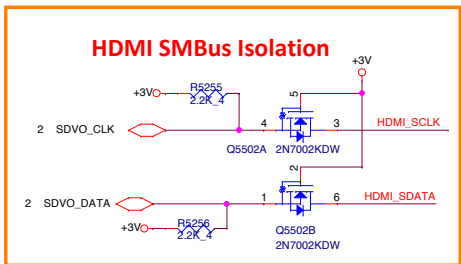
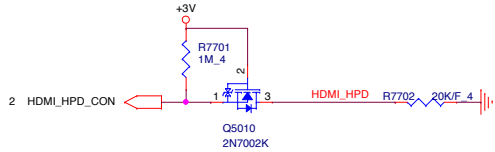
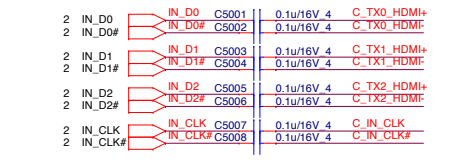
Reserve for codec debug

Mute LED改用Mic2-Vref0-R  
Mic偏壓改用Mic2-Vref0-L

place to under codec

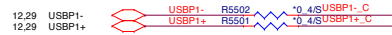
PROJECT : NFLP\_KBLU\_DR  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	28 -- Codec ALC3258-CG	1A
Date: Friday, March 24, 2017	Sheet 26 of 49	

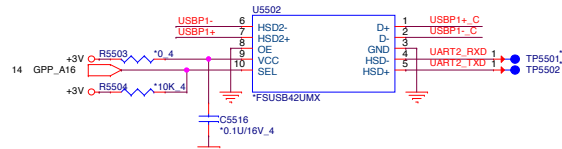


Head Phone out

	<b>PROJECT : NFLP_KBLU_DR</b> Quanta Computer Inc.		
	Size C	Document Number <b>30 - LAN RTL8107EH/RTL8111HS</b>	Rev 1A
Date: Friday, March 24, 2017	Sheet 28 of 49		



## UART for Win7 WHQL DEBUG



Place Back to Back La

## USB3.0

reserve for re-driver un-stuff 01/18

## USB3.0

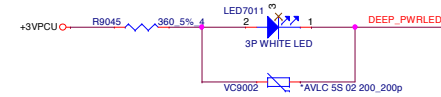
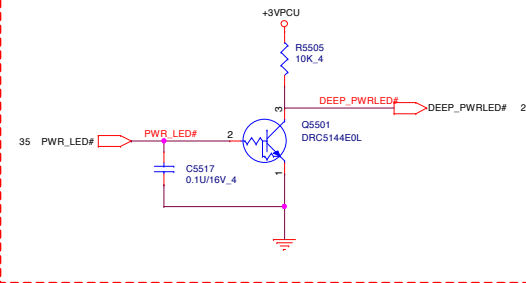
reserve for re-driver un-stuff 01/18

Layout Notes:  
Stubs Trace less than 150mil

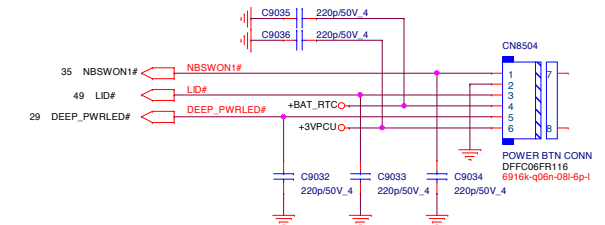
Layout Notes:  
Stubs Trace less than 150mil

## Daughter Board

1123 Add PWR LED MOS Circuit

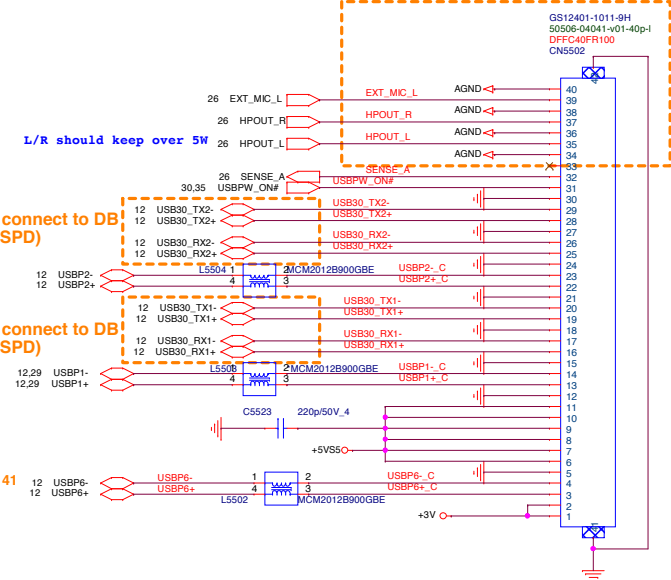


## Power Board



## Daughter Board

For Audio layout routing



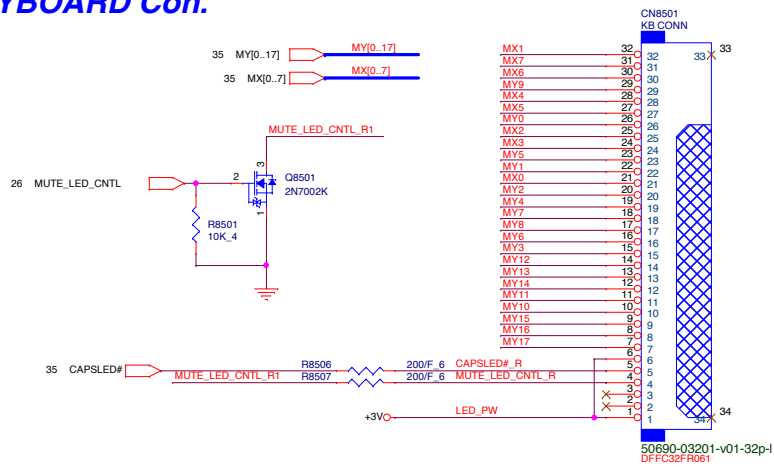
**PROJECT : NFLP\_KBLU\_DR**  
Quanta Computer Inc.

Size Custom	Document Number	Rev 1A
	<b>31 - USB SW &amp; TYPE-C -TPS25810</b>	
Date: Friday, March 24, 2017	Sheet 29 of 49	

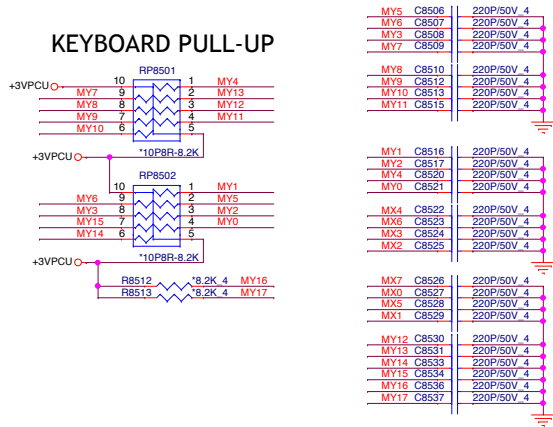




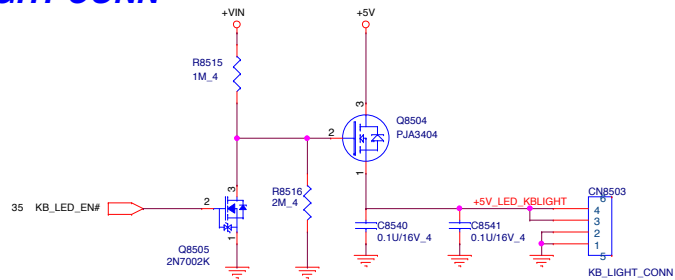
## KEYBOARD Con.



### KEYBOARD PULL-UP

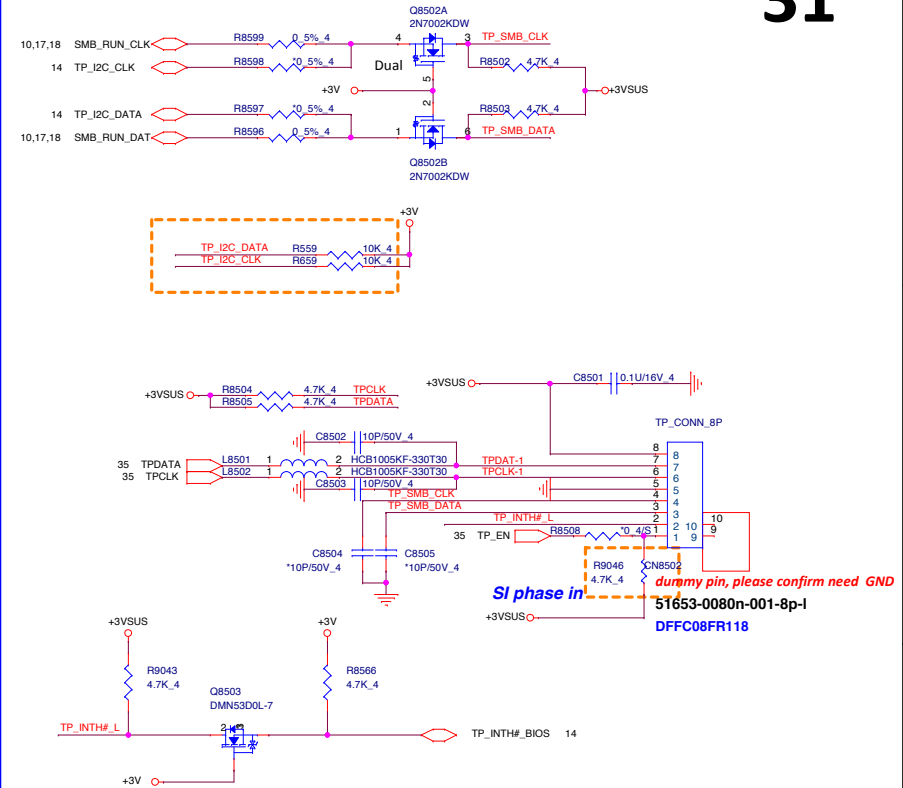


## KB LIGHT CONN

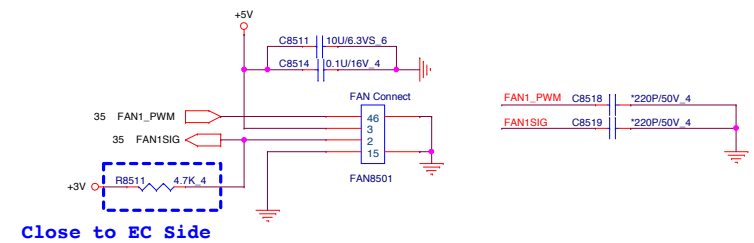


## Touch Pad Connector

31

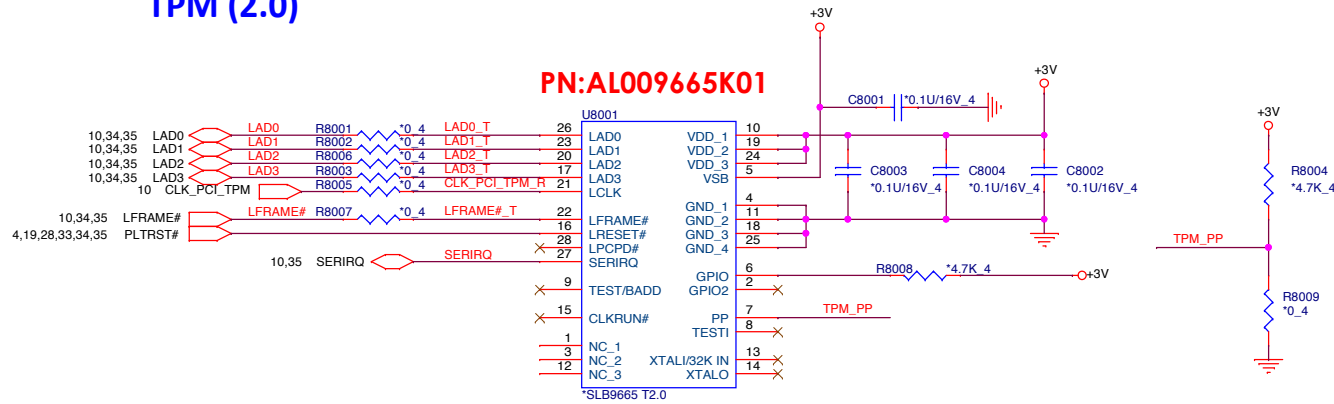


## FAN

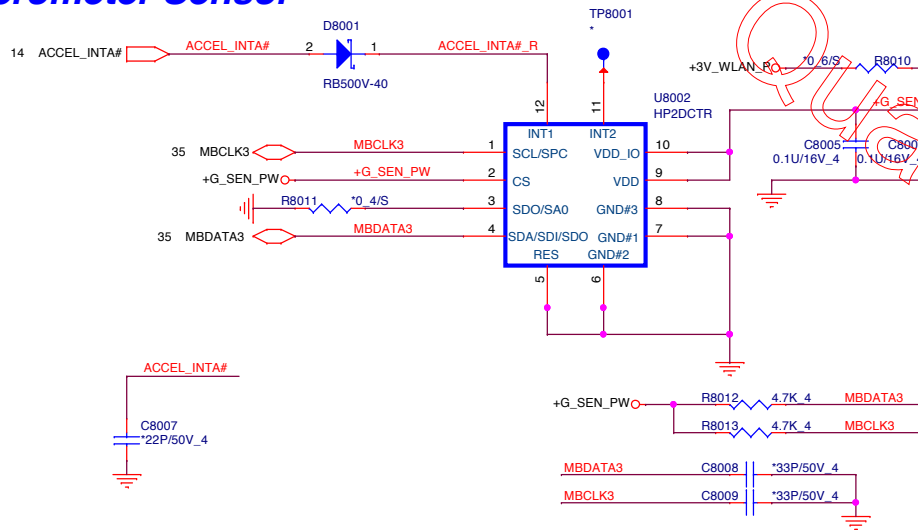


## TPM (2.0)

32

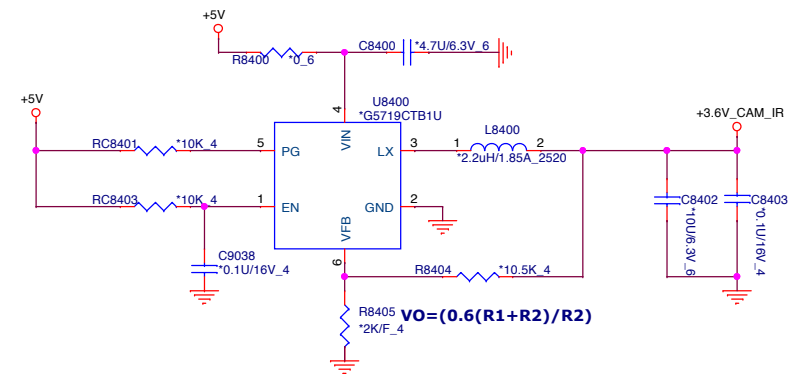
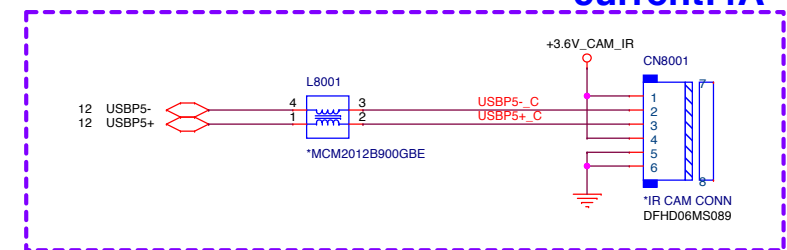


## Accelerometer Sensor



## IR CAM

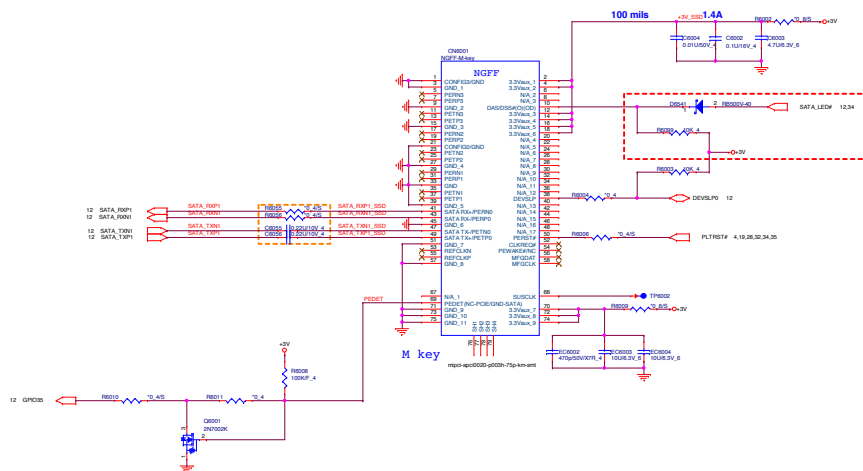
current:4A



**PROJECT : NFLP\_KBLU\_DR**  
Quanta Computer Inc.

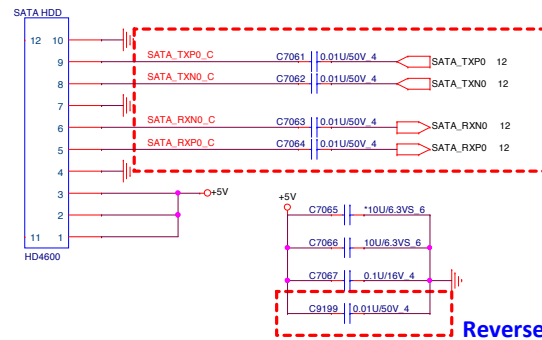
Size Custom	Document Number <b>34 -- TPM/G-Sensor/IR CAM</b>	Rev 1A
Date: Friday, March 24, 2017	Sheet	32 of 49

## 33

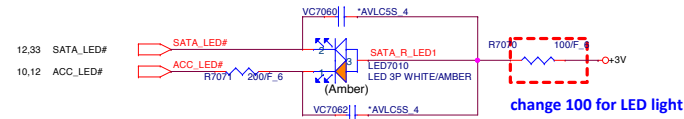


eMMC

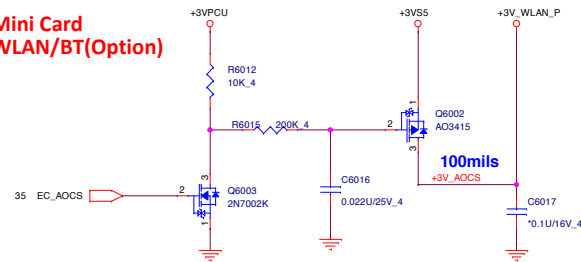
## SATA HDD



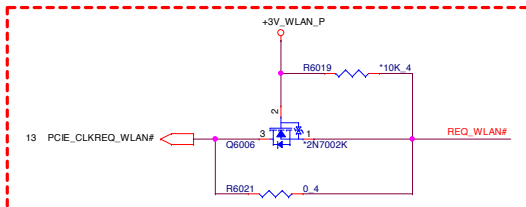
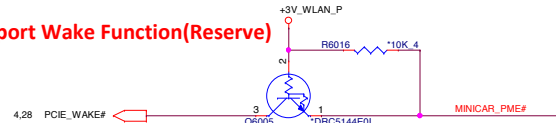
## SATA LED



## WLAN

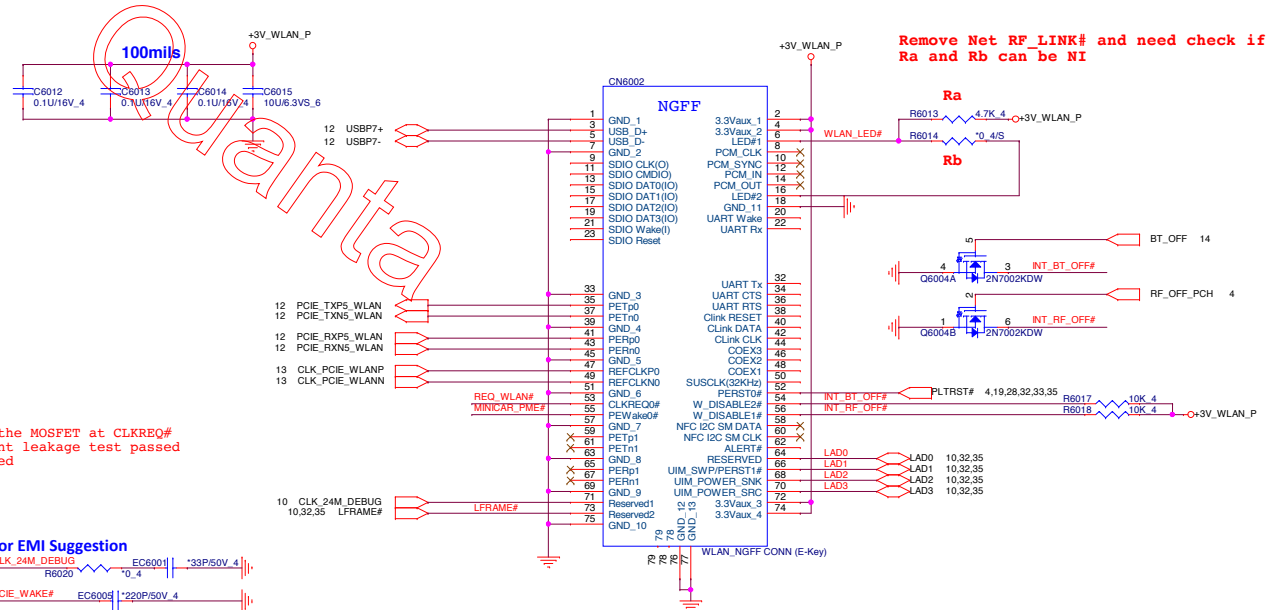
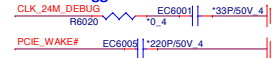
Mini Card  
WLAN/BT(Optional)

## Support Wake Function(Reserve)



0302 Reserved the MOSFET at CLKREQ#  
even the current leakage test passed  
for HP requested

## For EMI Suggestion



PROJECT : NFLP\_KBLU\_DR  
Quanta Computer Inc.

Size: Custom  
Document Number: 36 -- HDD/WLAN(NGFF)  
Date: Monday, March 27, 2017  
Sheet: 34 of 49  
Rev: 1A



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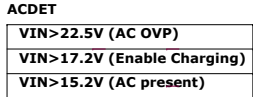
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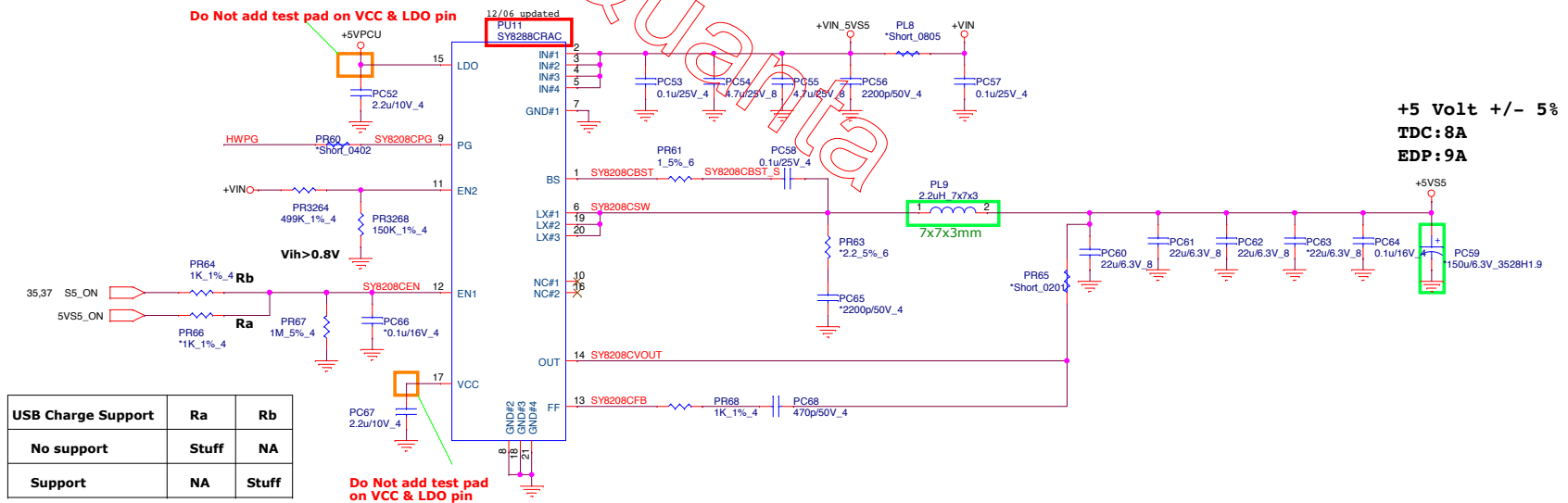
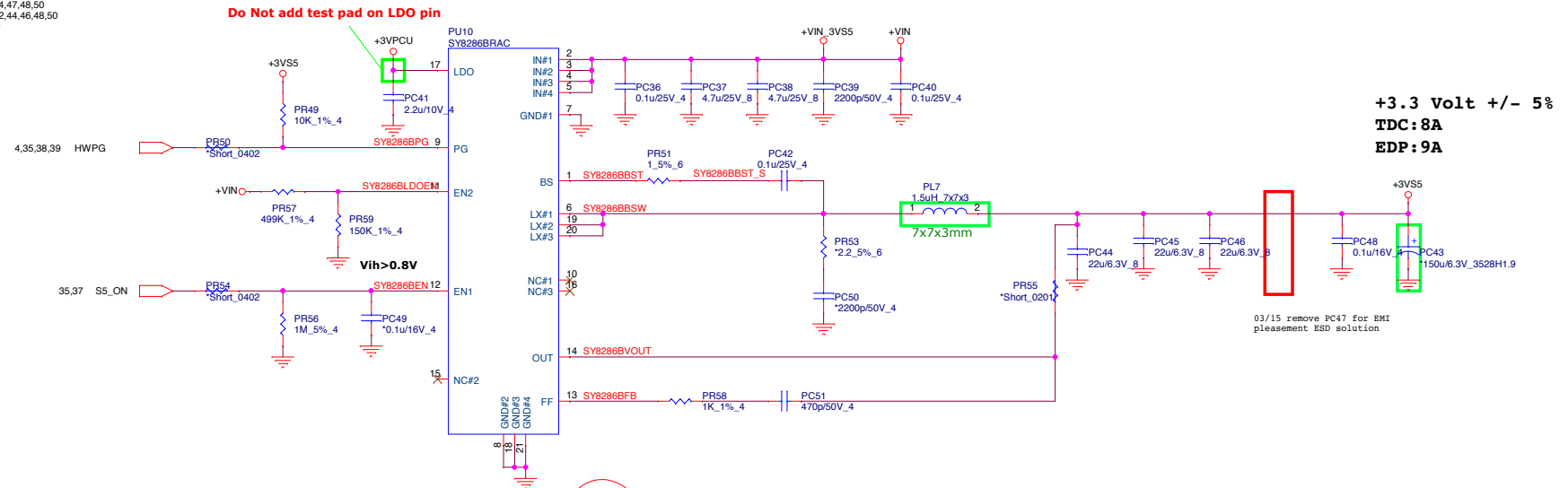
**3S1P 41Whr**

 <b>BU5</b>	<b>PROJECT : NFLP_KBLU_DR</b> Quanta Computer Inc.		
	Size Custom	Document Number <b>Charger (BQ24738H)</b>	Rev 1A
Date <u>Friday, March 24, 2017</u>		Sheet <u>36</u> of <u>51</u>	

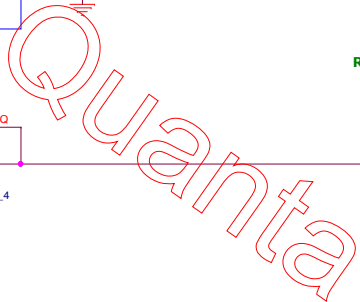


**DC/DC +3VS5/+5VS5**

	+VIN	25,31,36,38,39,42,43,44,45,46,50
	+3VS5	4,10,15,25,34,35,38,39,40,44,47,48,50
	+5VS5	4,25,26,29,30,38,39,40,41,42,44,46,48,50
	+3VPCU	6,13,29,30,31,34,35,36,49
	+5VPCU	26,36,47,48



<b>USB Charge Support</b>	<b>Ra</b>	<b>Rb</b>
<b>No support</b>	<b>Stuff</b>	<b>NA</b>
<b>Support</b>	<b>NA</b>	<b>Stuff</b>

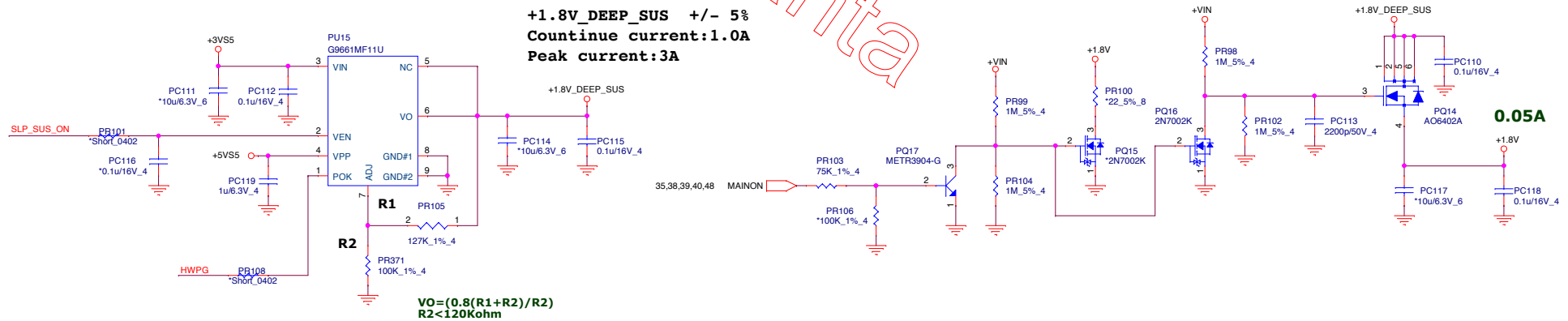
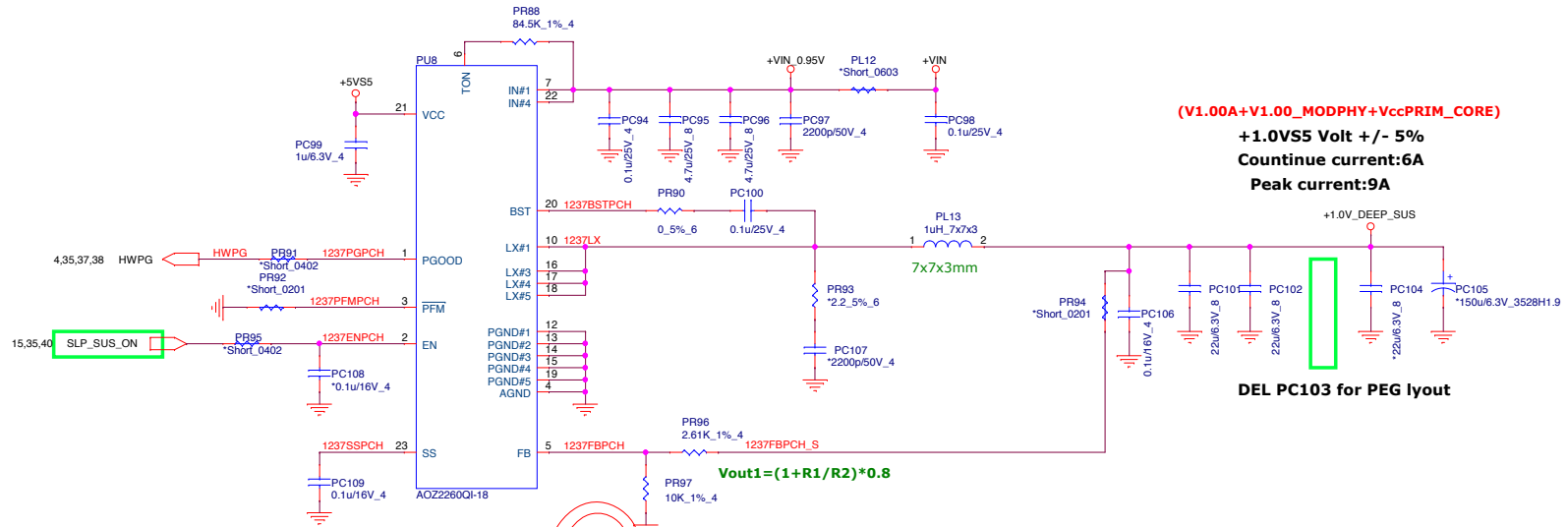


**+2.5VSUS +/- 3%**  
**Continuous current:2A**  
**Peak current:3A**  
**OCp minimum:4A**

The diagram shows a voltage regulator (PU13, G9661MF11U) with the following components and connections:

- Input:** VIN (pin 3) is connected to a +3VS5 input through capacitor PC88 (10u/6.3V\_6). VEN (pin 2) is connected to a +5VS5 input through capacitor PC92 (0.1u/16V\_4).
- Grounding:** GND#1 (pin 8) and GND#2 (pin 9) are connected to ground through capacitor PC93 (1u/6.3V\_4).
- Output:** VO (pin 6) is connected to a +2.5VSUS output through capacitor PC90 (10u/6.3V\_6).
- Feedback:** The ADJ (pin 7) pin is connected to a voltage divider consisting of resistors R1 (215K\_1%\_4) and R2 (100K\_1%\_4) connected to ground.
- Other Connections:** POK (pin 1) is connected to a +5VS5 input through capacitor PC93 (1u/6.3V\_4). The NC (pin 5) pin is connected to ground through capacitor PC91 (0.1u/16V\_4).
- Labels:** The input is labeled SUSON and the output is labeled HWPG.

+VIN 25,31,36,37,38,42,43,44,45,46,50  
 +3VS5 4,10,15,25,34,35,37,38,40,44,47,48,50  
 +5VS5 4,25,26,29,30,37,38,40,41,42,44,46,48,50  
 +1.0V\_DEEP\_SUS 9,13,15,40  
 +1.8V\_DEEP\_SUS 9,15,47  
 MAINON 35,38,39,40,48  
 +1.5V

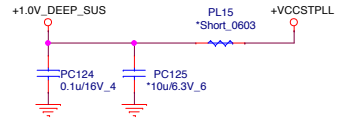


+1.0V 2,4,6,35  
 +3VSS 4,10,15,25,34,35,37,38,39,44,47,48,50  
 +5VSS 4,25,28,29,30,37,38,39,41,42,44,46,48,50  
 +VCCIO 2,6  
 +1.2VSUS 3,6,17,18,38  
 +VCCSTPLL 2,4,5,6,9,41  
 +1.0V\_DEEP\_SUS 9,13,15,39  
 +1.2V\_VCCPLL\_OC 6  
 MAINON 35,38,39,48

**Volume Segment**  
**Vcc\_ST: 0.12A**  
**Vcc\_PLL: 0.12A**

**<= 10ms, full load ready**  
**(Vcc\_ST+Vcc\_PLL)**

**Imax:0.24A**

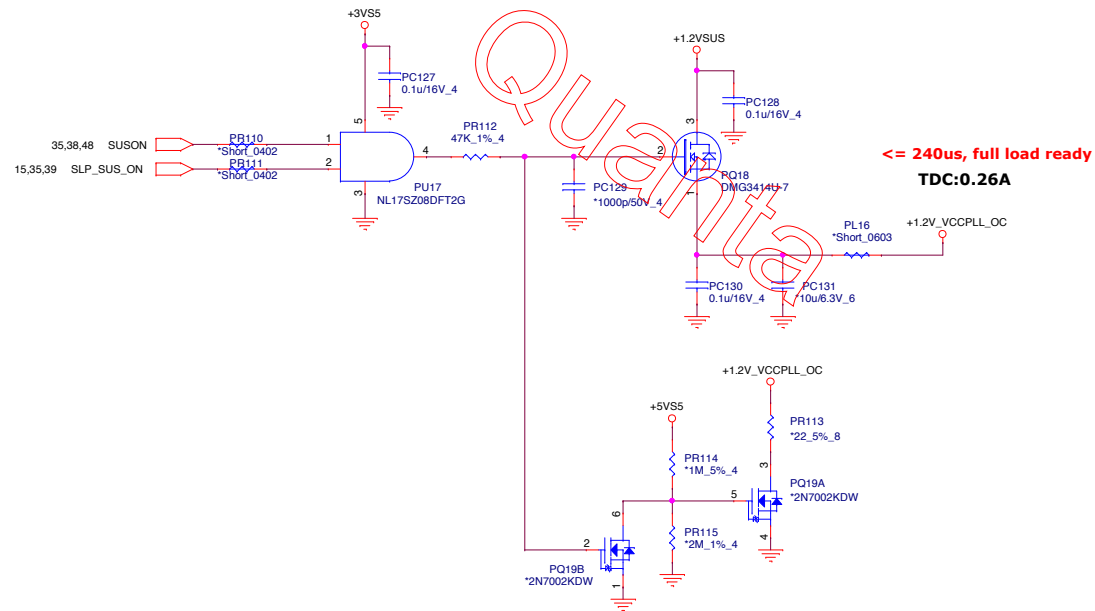
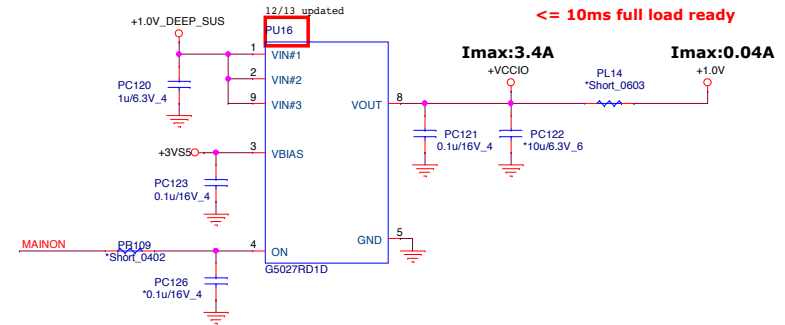


**Volume Segment**  
**Vcc\_STG: 0.04A**  
**Vcc\_IO: 3.4A**

**<= 10ms full load ready**

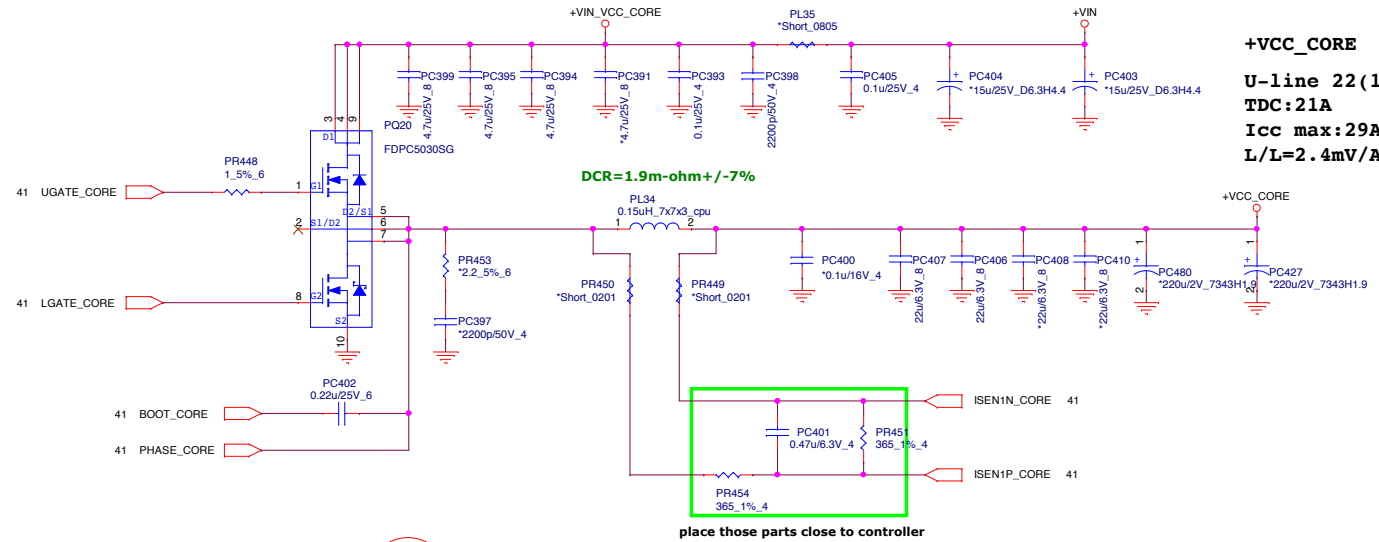
**Imax:3.4A**

**Imax:0.04A**

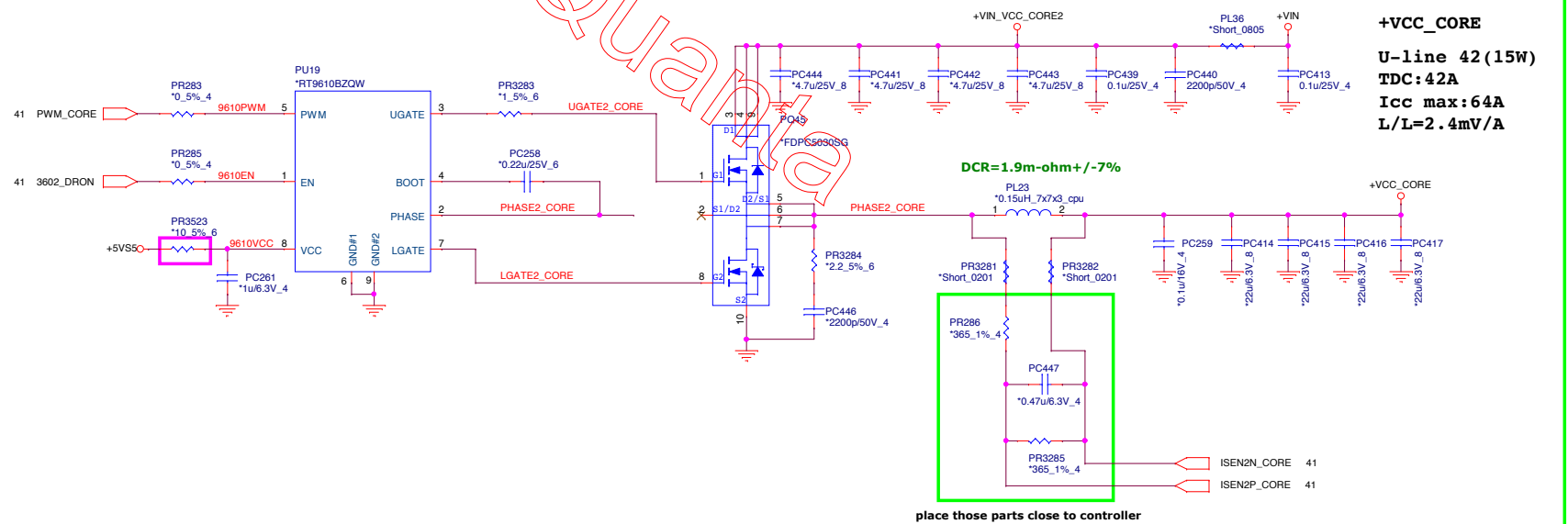




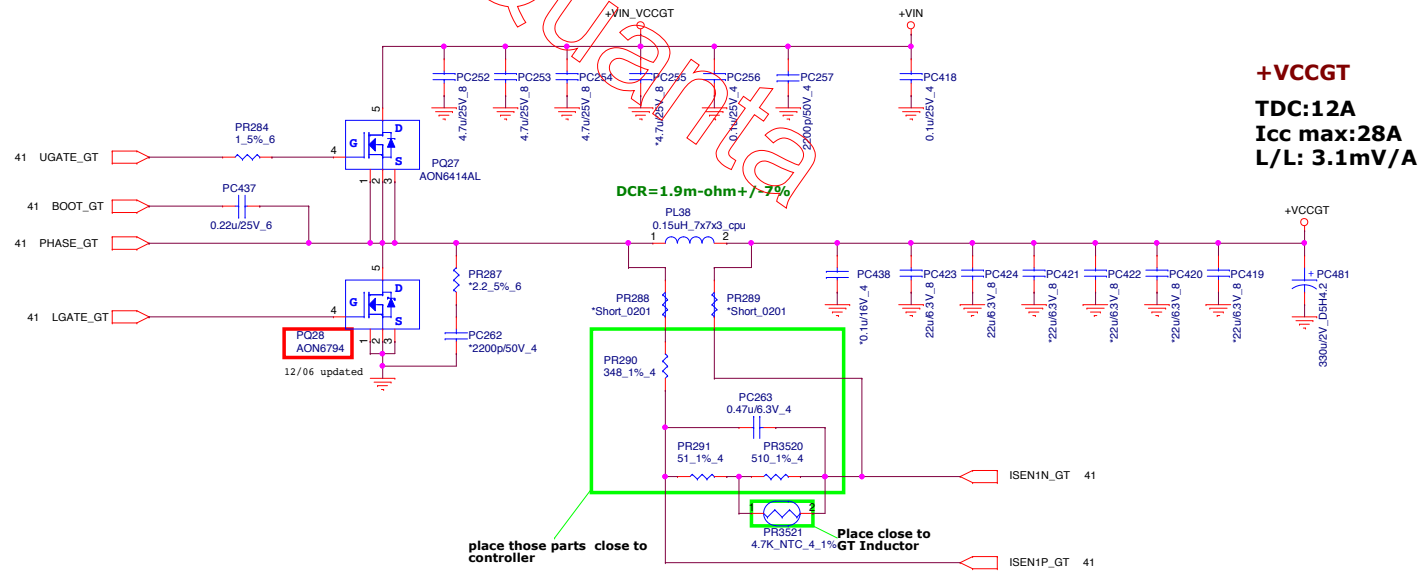
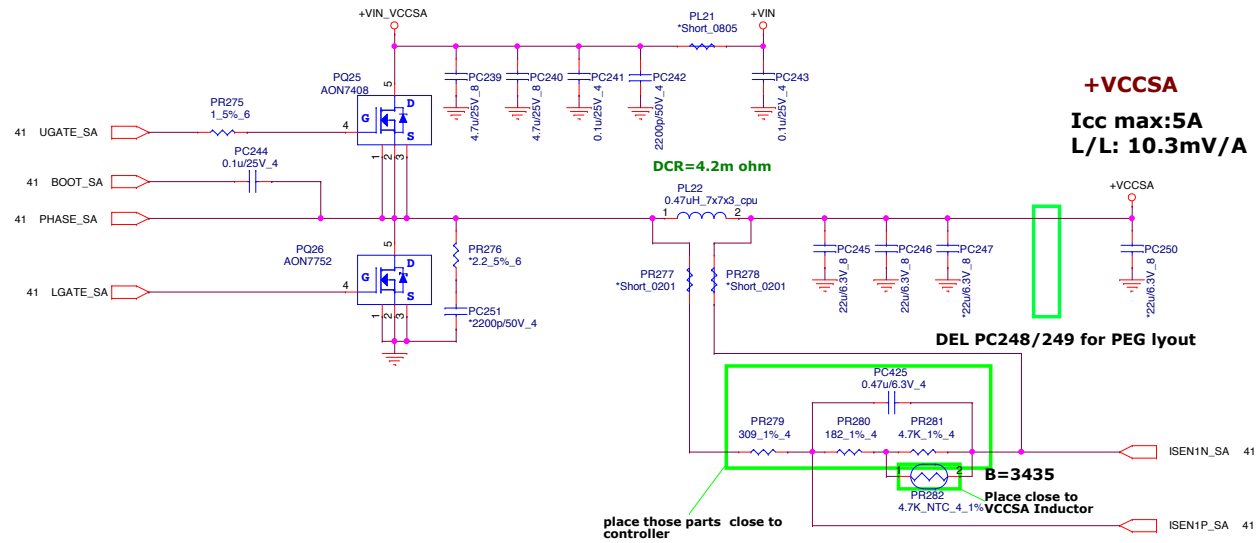
+VIN 25,31,36,37,38,39,43,44,45,46,50  
+5VSS 4,25,26,29,30,37,38,39,40,41,44,46,48,50



For U42 --> Add These Components



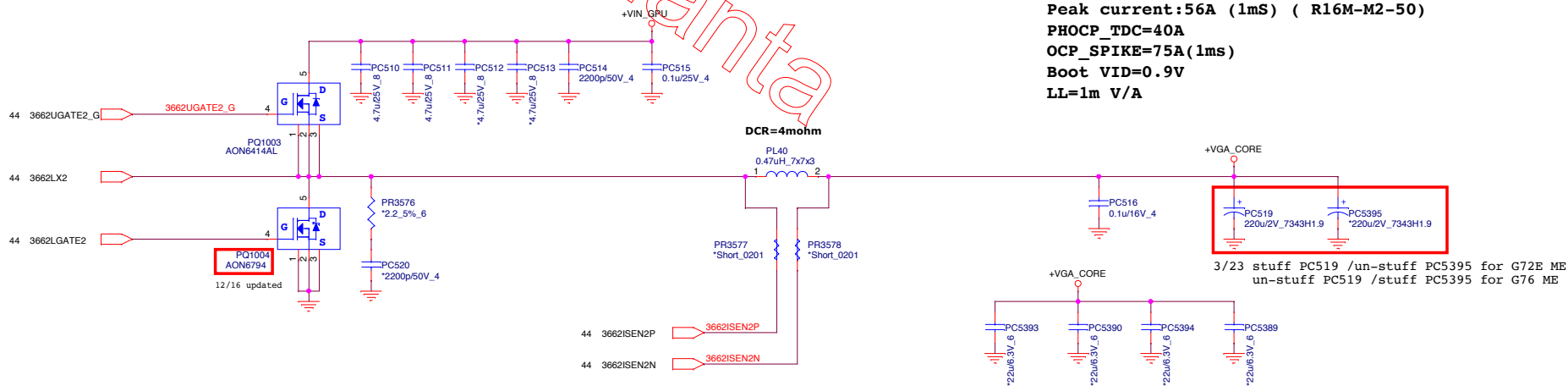
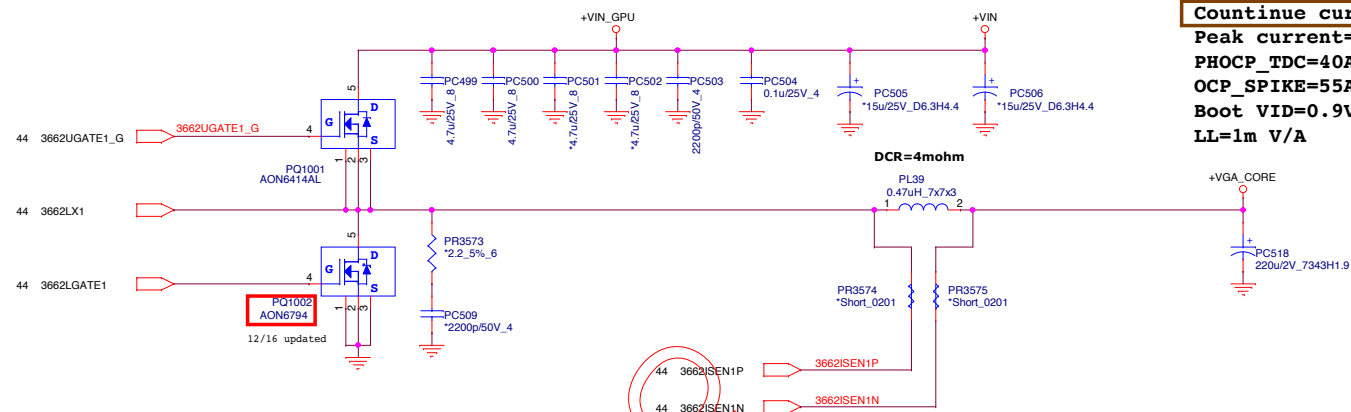
+VIN 25,31,36,37,38,39,42,44,45,46,50  
 +5VS5 4,25,26,29,30,37,38,39,40,41,42,44,46,48,50  
 +VCCSA 6,41  
 +VCCGT 7,41

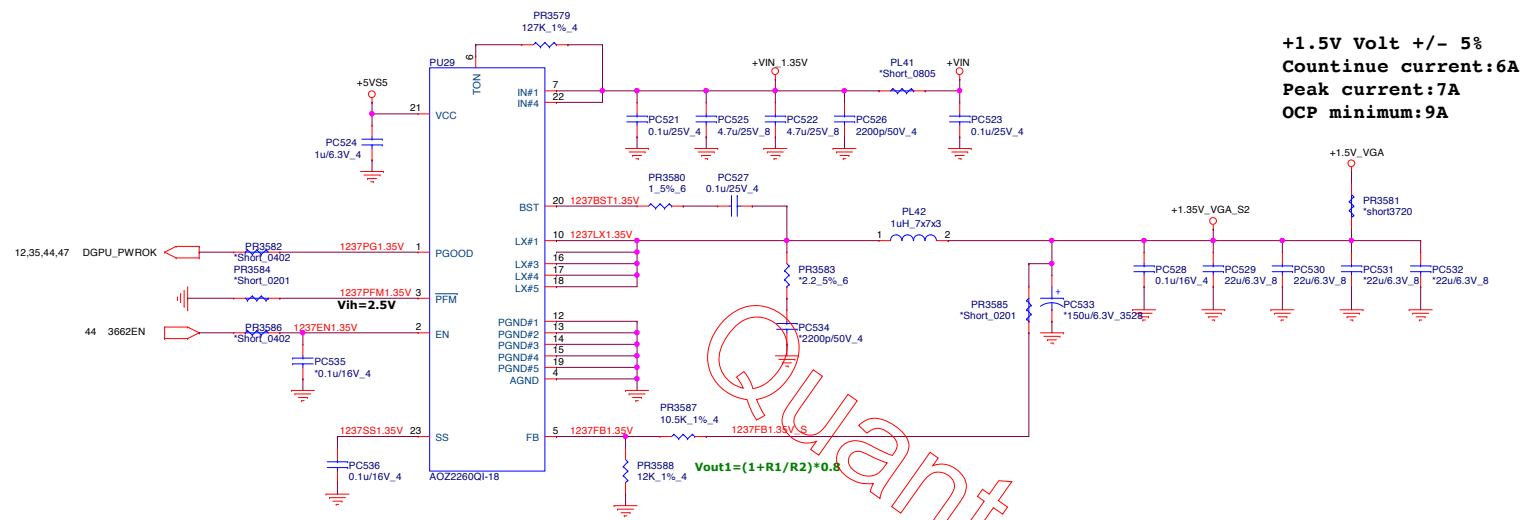




	1 Phase setting	
R1		
R2		
R3		

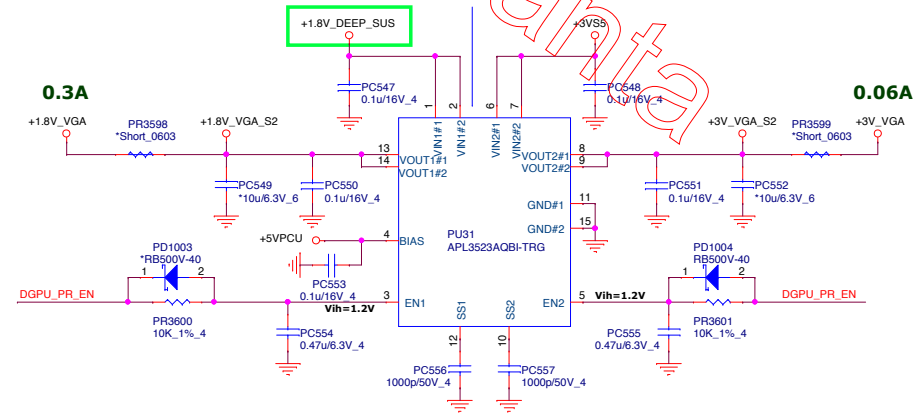
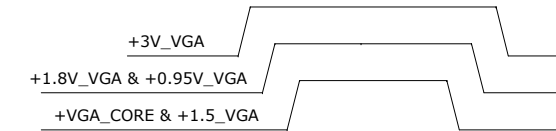
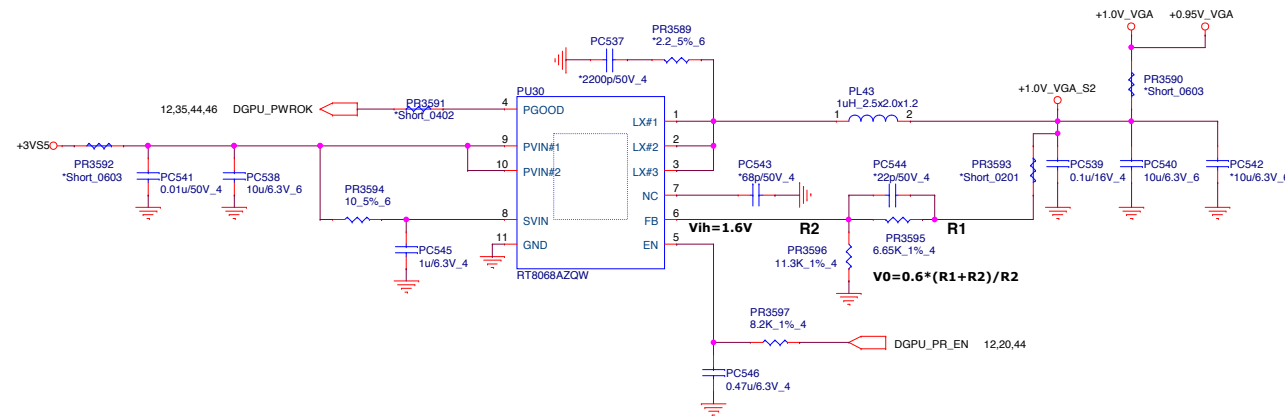
	1 Phase setting	
R4		



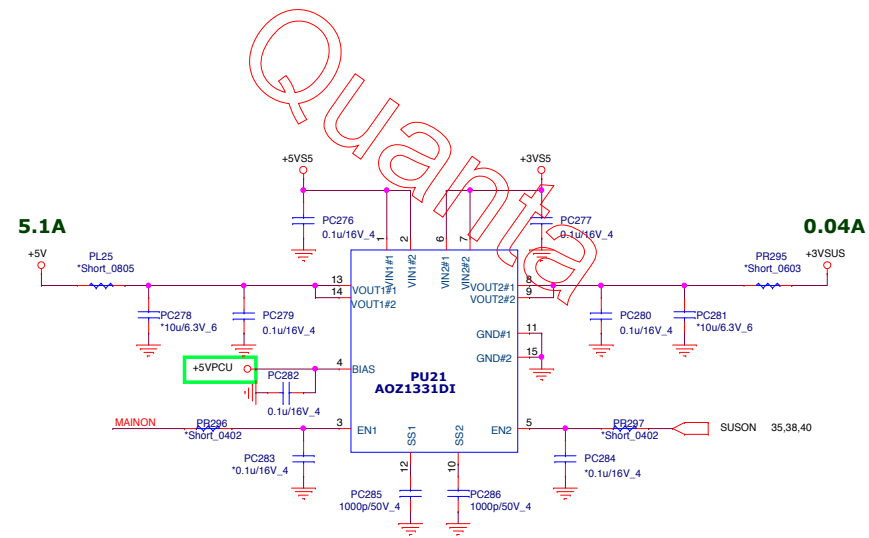
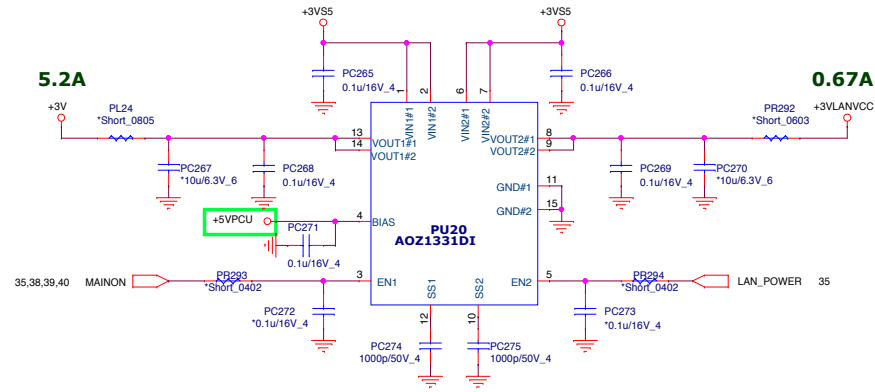


Vo	Rton
0.95V	82k
1V	84.5k
1.05V	95.3k
1.35V	113k
1.5V	127k

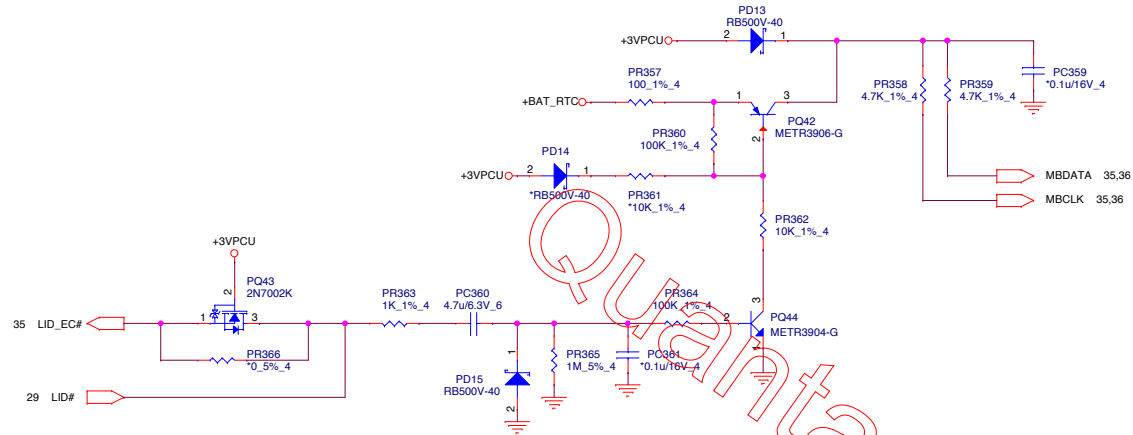
**+0.95V +/- 3%**  
**Countinue current:2A**  
**Peak current:3A**  
**OCP minimum:4A**



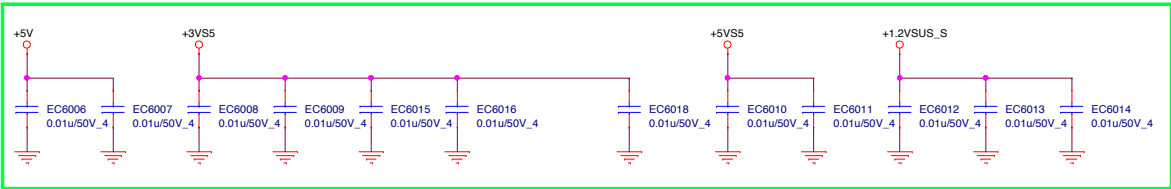
+3V	2,4,10,11,12,13,14,15,17,18,25,26,27,28,29,31,32,33,34,35,41
+5V	25,26,27,31,32,34,50
+VIN	25,31,36,37,38,39,42,43,44,45,46,50
+3VS5	4,10,15,25,34,35,37,38,39,40,44,47,50
+5VS5	4,25,26,29,30,37,38,39,40,41,42,44,46,50
+3VSUS	31
+5VPCU	26,36,37,47
+3VLAVCC	28



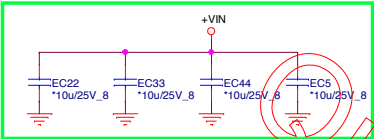
+3VPCU 6,13,29,30,31,34,35,36,37  
+BAT\_RTC 4,13,15,29,36



EMI request for ESD 03/21 updated



EMI request for ISN



EMI request for ISN

